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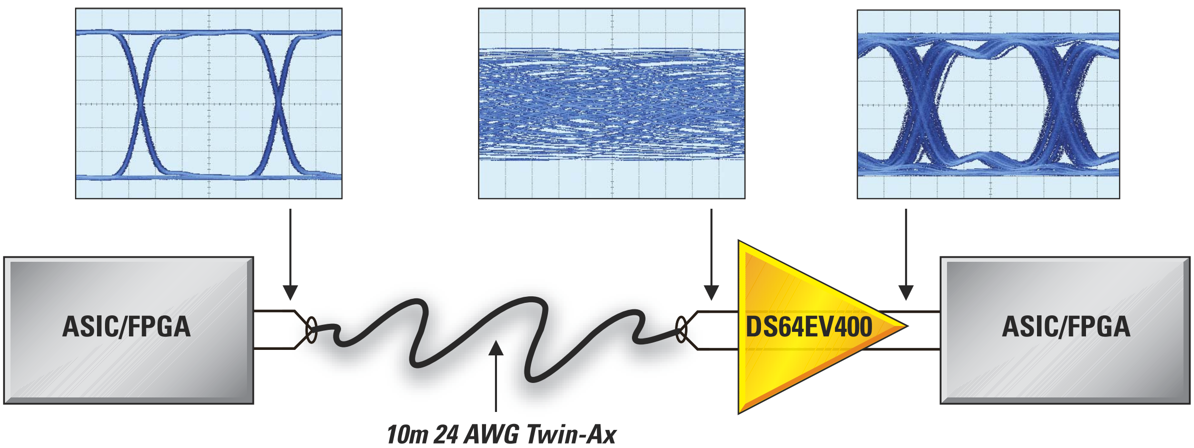

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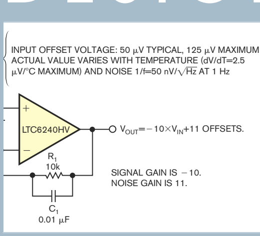

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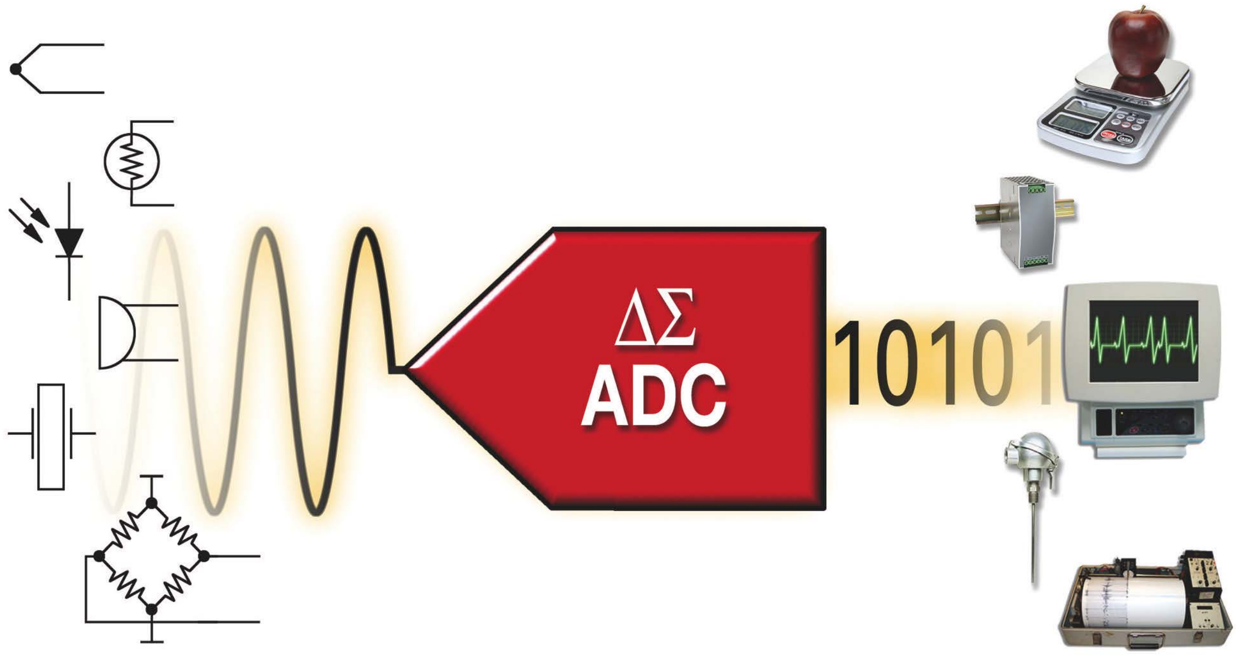

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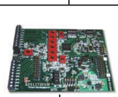

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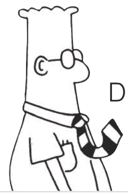

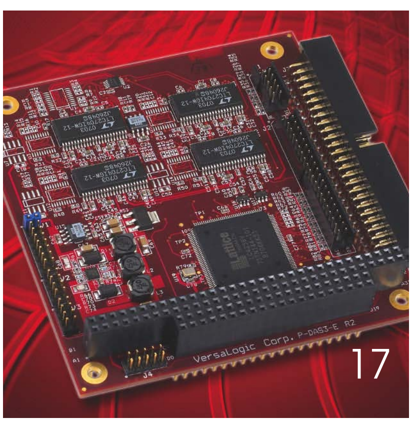

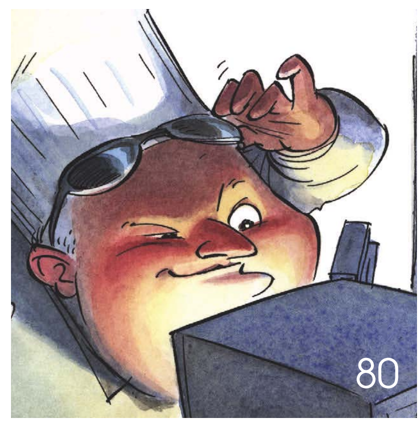

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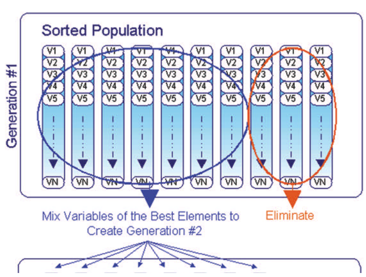

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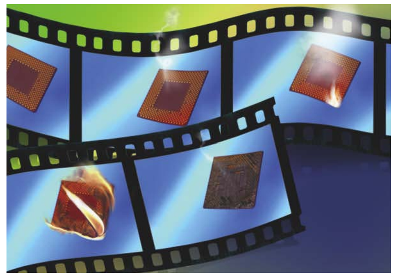

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AWARD WINNER

Congratulations to Senior Technical Editor Brian Dipert, winner of a 54th Annual Jesse H Neal National Business Journalism Award for his blog, *Brian's Brain*. The Neal Awards are among the most prestigious and sought-after editorial honors. The awards committee described *Brian's Brain* as "a rare combination of authoritative tech argument and a clear connection to the business community." Check it out for yourself.
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FROM *EDN*'S BLOGS

Laptop catches fire, but don't blame the battery just yet
From PowerSource, by Margery Conner
Before fingering the lithium-ion chemistry as being faulty, consider that the laptop apparently was sitting on a blanket on an upholstered loveseat, making it likely that the air vents were blocked. Especially for battery-powered designs, this is a good reminder that available ambient air can vary greatly.
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BY KAREN FIELD, EDITORIAL DIRECTOR

Hello, *EDN* readers!

As a former design engineer at Texas Instruments and, as a reader of this magazine, I can't tell you how excited and proud I am to join the team here at *EDN* as the new editorial director. From the enduringly popular Design Ideas and deep technical articles to new online offerings such as Video Design Ideas and blogs including Senior Technical Editor Brian Dipert's *Brian's Brain* and Technical Editor Paul Rako's *Anablog*, it's clear that *EDN*'s editors are committed to delivering the most compelling, useful, and unique content for design engineers. I love that about *EDN*.

In the future, you can expect to continue to get all the things that you love from *EDN*—and more. In my new role, I'll be working with the editorial team to develop innovative content that you won't be able to find anywhere else. Currently, we're exploring different ways to create and present content that's highly relevant and useful to design engineers, including video, flash animation, photo galleries, and searchable databases. We're also committed to in-depth coverage of the topics that you tell us are of highest interest and importance, such as development kits and tools.

In a recent survey of *EDN* readers, 95% of the respondents reported that they bought at least one development kit in the past year. Most bought more than one, with some 10% reporting that they'd purchased five or more kits last year. Development-kit sales in general are up, with some vendors noting increases of 50 to 100% over the past three years. You may wonder why a flurry of interest in development kits has suddenly occurred. With never-ending pressure to quickly get their designs out the door—and you know this better than I—design engineers increasingly use development kits and boards to prove a concept, learn about software tools, quickly build a prototype, avoid building a PCB (printed-circuit board), and test and evaluate their designs.

In turn, manufacturers and third-party makers have increased their kit offerings, focusing on ease of use, better documentation, and greater performance. And it's no wonder that they're taking these steps: The stakes are huge. They know that there's a high probability that, when engineers have a good experience with a development kit, they'll spec the component into the final design.

The same survey revealed that you not only use a lot of these kits, but also want more information on them, including reviews of kits by engineers who have used them, and an easier way to find information on them. So, I'm pleased to announce that, in response to your wish list, *EDN* has created the *Devmonkey* Web site (www.developmentmonkey.com). We launched it on Feb 1, 2008, and it is the first Web site to focus exclusively on the latest news and information on development tools for design engineers. Here, you will find the most up-to-date articles on new kits and tools, as well as hands-on reviews of some of the latest kits from our Senior Reviews Editor Jon Titus. A former editor at *EDN*, he's been reviewing kits for years and has unique access to the companies and application engineers who develop them. He also writes the *Devmonkey* blog for the Web site, in which he previews new goodies coming down the pipeline and tips and tricks based on his own experiences with development kits and tools.

A new form of content on the site is our two-minute demo videos, in which Titus reviews kits and describes their key features and capabilities. He also talks about what he's done with a kit that goes beyond the basic documentation. This year, we'll add even more content to the site, including kit reviews from readers and gadgets our readers have designed using a kit. If you have a moment, please check out the *Devmonkey* site. I'd love to get your feedback on the site and on the sorts of features you find most valuable. Please drop me a line at kfield@reedbusiness.com. You can also sign up for the *EDN* e-newsletter on development tools, which brings you the latest *Devmonkey* content each month. To subscribe, go to www.edn.com and click on the "Free e-mail newsletters" button in the upper right corner.

And stay tuned. We have a slew of new ideas in the pipeline that we expect to introduce in the coming year that we hope you're going to like a lot. **EDN**

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ANALOG edge℠

Design Considerations for a Transimpedance Amplifier

Application Note AN-1803

Maithil Pachchigar, Applications Engineer

It's challenging to design a good current-to-voltage (transimpedance) converter using a Voltage-Feedback Amplifier (VFA). By definition, a photodiode produces either a current or voltage output from exposure to light. The Transimpedance Amplifier (TIA) is utilized to convert this low-level current to a usable voltage signal and the TIA often needs to be compensated for proper operation. This article explores a simple TIA design using a 345 MHz rail-to-rail output VFA, such as National's LMH6611. The main goal of this article is to offer necessary information for TIA design, discuss TIA compensation and performance results and analyze the noise at the output of the TIA.

A voltage feedback amplifier modeled as a TIA with photodiode and the internal op amp capacitances is illustrated in ***Figure 1***.

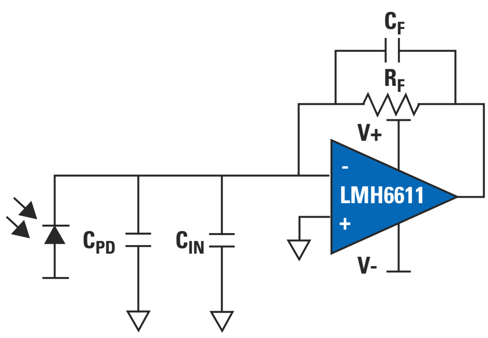

Figure 1. Photodiode Modeled with Capacitive Elements

The LMH6611 allows circuit operation of a low light intensity due to its low-input bias current by using larger values of gain (R_F). The total capacitance (C_T) on the inverting terminal of the op amp includes the photodiode capacitance (C_{PD}) and the input capacitance (C_{IN}). The C_T plays an important role in the stability of the circuit. The Noise Gain (NG) of this circuit determines the stability, and is defined by:

$$NG = \frac{1 + sR_F\,(C_T + C_F)}{1 + sC_FR_F} \qquad \textit{Equation 1}$$

Where $f_Z \cong \dfrac{1}{2\pi R_F C_T}$ *Equation 2*

Figure 2 shows the bode plot of the noise gain intersecting the op amp open-loop gain (A_{OL}). With larger values of gain (R_F), C_T and R_F create a zero in the transfer function. At higher frequencies, transimpedance amplifiers could become inherently unstable as there will be excess phase shift around the loop.

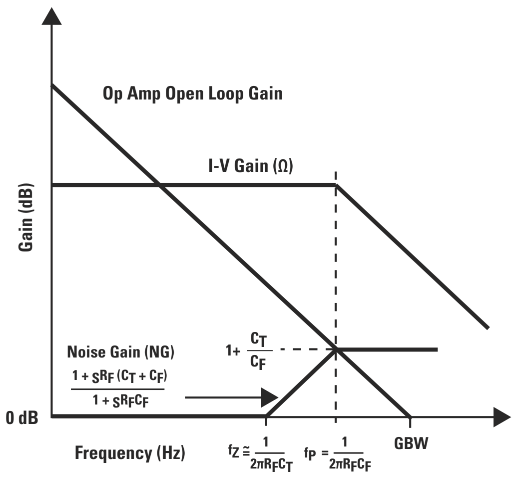

Figure 2. Bode Plot of Noise Gain Intersecting with Op Amp Open-Loop Gain

In order to maintain the stability, a feedback capacitor (C_F) across R_F is placed to create a pole at f_P in the noise gain function. The noise gain slope will be flattened by choosing an appropriate value of C_F for the optimum performance, such that noise gain is equal to the open loop gain of the op amp at f_P. This "flattening" of the noise gain slope beyond the point of intercept of A_{OL} and noise gain will result in a Phase Margin (PM) of 45°. Because at the point of intercept, the noise gain pole at f_P will have a 45° phase lead contribution that gives PM of 45° (assuming f_P and f_Z are at least a decade apart).

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Equations 3 and *4* theoretically calculate the optimum value of C_F and the expected -3 dB bandwidth:

$$C_F = \sqrt{\frac{C_T}{2\pi R_F(GBW)}} \quad \textit{Equation 3}$$

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi C_T R_F}} \quad \textit{Equation 4}$$

Equation 4 indicates that the -3 dB bandwidth of the TIA is inversely proportional to the feedback resistor. Therefore, if the bandwidth is important, then the best approach would be to have a moderate transimpedance gain stage followed by a broadband voltage gain stage.

Table 1 shows the measurement results of the LMH6611 with different photodiodes having various capacitances (C_{PD}) at a transimpedance gain (R_F) of 1 kΩ. The C_F and f_{-3dB} values are calculated from the *Equations 3* and *4* respectively.

Table 1. TIA (Figure 1) Compensation and Performance Results

C_{PD} (pf)	C_T (pf)	C_F CAL (pf)	C_F USED (pf)	$f_{-3\,dB}$ CAL (MHz)	$f_{-3\,dB}$ Meas (MHz)	Peaking (dB)
22	24	5.42	5.6	29.3	27.1	0.5
47	49	7.75	8	20.5	21	0.5
100	102	11.15	12	14.2	15.2	0.5
222	224	20.39	18	9.6	10.7	0.5
330	332	20.2	22	7.9	9	0.8

Note:
Vs= +/-2.5V
GBW = 130 MHz
$C_T = C_{PD} + C_{IN}$
C_{IN} = 2 pf

Figure 3 shows the frequency response for the various photodiodes used in *Table 1*. The signal-to-noise ratio is improved when all the required gain is placed in the TIA stage, because the noise spectral density produced by R_F increases with the square-root of R_F and the signal increases linearly.

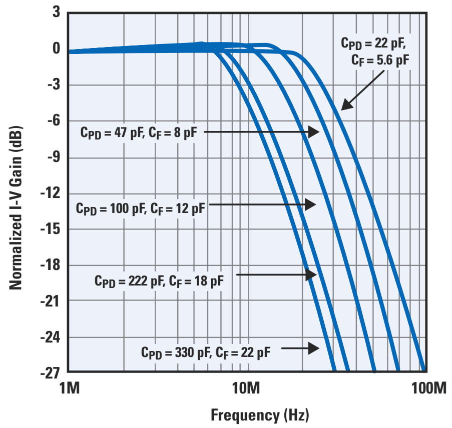

Figure 3. Frequency Response of the LMH6611 for the Various Photodiodes

It is essential to take into account various noise sources. Op amp noise voltage, feedback resistor thermal noise, input noise current, and photodiode noise current do not all operate over the same frequency range while analyzing the noise at the output of the TIA. The op amp noise voltage will be gained up in the region between the noise gain's zero and its pole. The higher the values of R_F and C_T, the sooner the noise gain peaking starts, and therefore its contribution to the total output noise will be larger. An equivalent total-noise voltage is computed by taking the square root of the sum of squared contributing noise voltages at the output of TIA.

To summarize, the total capacitance (C_T) plays an important role in the stability of the TIA and hence it is advantageous to minimize C_T by proper op amp choice, or by applying a reverse bias across the diode at the expense of excess current and noise. This article has also shown that various photodiodes and the compensation method used in the lab confirm a good match between the theory and the bench measurements.

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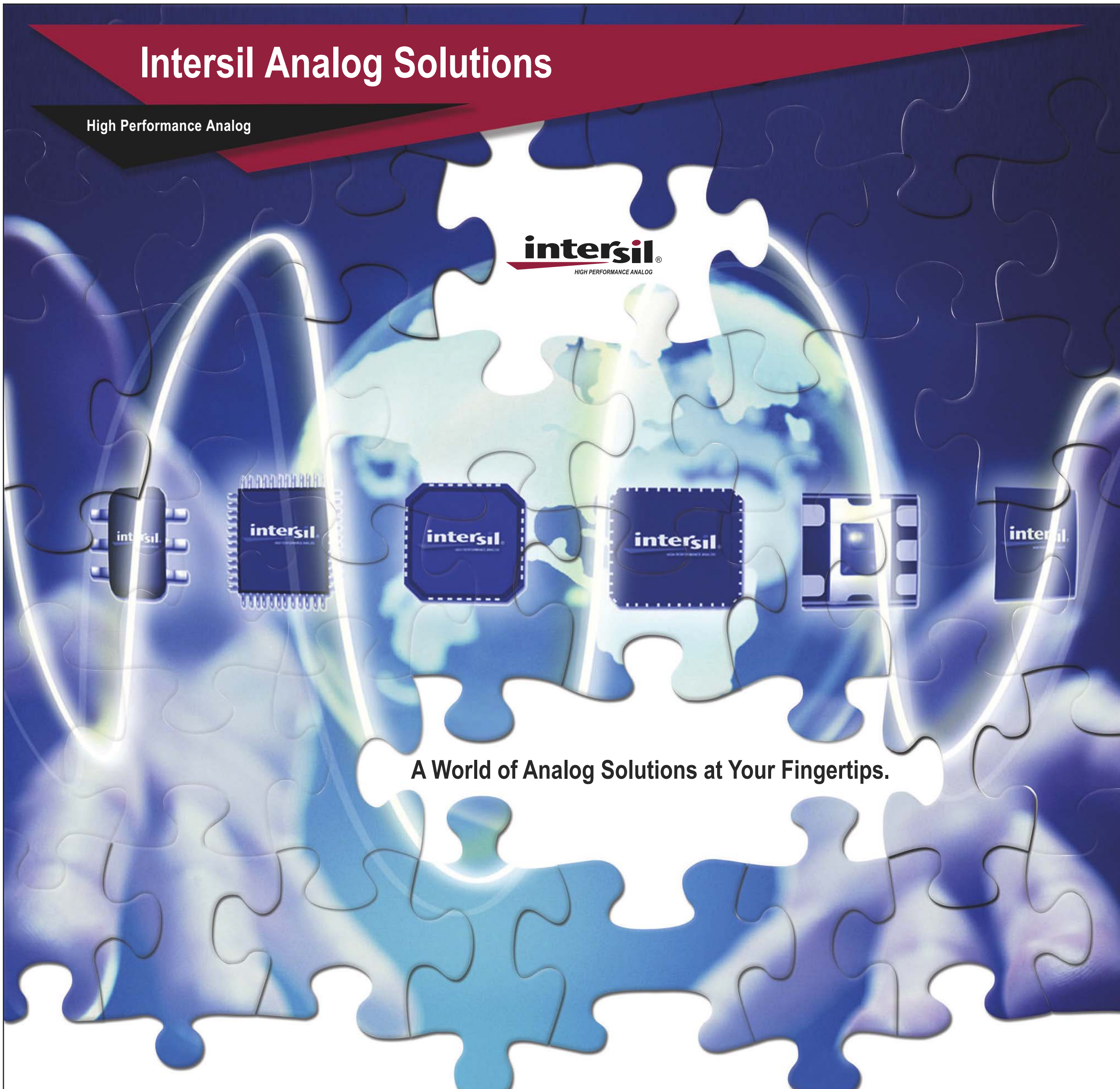

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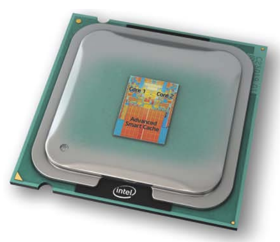
Intel launches 45-nm quad- and dual-core processors for embedded-system applications

Intel Corp is shipping quad- and dual-core processors that the company based on its high-k-metal-gate-transistor formula and manufactured on its 45-nm process. The new processors, which include the quad-core Xeon 5400 series and the dual-core Xeon 5200 series combine with Intel's power-optimized 5100 memory-controller-hub chip set to create the first 45-nm CPU platforms for thermally constrained, bladed systems, according to the company. When using Intel's 5000P chip set, the 45-nm processors target high-performance, memory-intensive applications, such as storage, routers, security, and medical equipment, as well as communications applications, including IMS (Internet Protocol-multimedia) subsystems.



The quad-core Xeon 5400 series and the dual-core Xeon 5200 series combine with Intel's power-optimized 5100 memory-controller-hub chip set to create the first 45-nm CPU platforms for thermally constrained bladed applications.

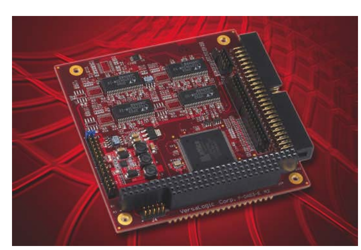
Intel claims that its hafnium-based, high-k-metal-gate-transistor formula reduces power consumption, increases switching speed, and offers greater transistor density than the company's 65-nm manufacturing technology. The 45-nm CPU-based platforms target a maximum power envelope of 200W, such as those for AdvancedTCA (Advanced Telecommunications Computing Architecture) and for NEBS (network-equipment-building-system) Level 3 requirements. Telecommunications company Ericsson (www.ericsson.com) plans to introduce its quad-core Xeon-processor-based IMS/core network nodes and application servers to allow operators and service providers to host more subscribers in a smaller footprint and to lower the total cost of ownership and environmental impact. The processing head room will also allow the development of the next generation of IMS services, according to Magnus Furustam, vice president and head of Ericsson's product-area core and IMS. To accelerate this innovation, Ericsson and Intel are promoting the benefits of IMS to the global communications-developer community.

Intel offers life-cycle support for seven years for the 5200 series, which includes the E5240, E5220, and L5238, and the 5400 series, which comprises the E5440 and L5408. This support represents a two-year increase from the previous minimum. The 45-nm processors with extended-life-cycle support are available now at prices of $321 to $690. The dual-core, 35W Xeon L5238 processor is now available, and the 5100 chip set, also available now, sells for $76.
—by Ann Steffora Mutschler
▷**Intel**, www.intel.com.

Analog-output module extends embedded I/O

Targeting applications such as process control, data monitoring and collection, security and medical-equipment design, VersaLogic's new VCM-DAS-3 PC/104 analog-output module offers a convenient and cost-effective method for adding I/O functions in single-board-embedded-computing applications. The ROHS-compliant PC/104 module features 16 channels of 12-bit analog output and 24 digital-I/O lines. In addition, the VCM-DAS-3 operates in an extended-temperature range of −40 to +85°C.

Enhanced features include independently programmable output ranges, software calibration, the ability to reset to zero scale on power-up, and readback of DAC and span codes for simplified setup. Legacy features include 8-bit-ISA (industry-standard-architecture)-bus compatibility, jumper-configurable output ranges in groups of eight, and the ability to reset to midscale on power-up. Prices for the DAS-3 start at approximately $400 (OEM quantities).**—by Warren Webb**
▷**VersaLogic Corp,** www.versalogic.com.



The PC/104 VCM-DAS-3 module features 16 channels of 12-bit analog output and 24 digital-I/O lines to support many embedded-computing applications.

pulse

Mixed-signal chip combines audio, power

Wolfson Microelectronics has introduced the AudioPlus product line, which will combine the company's expertise in high-quality audio for portable products with a power-management subsystem. Wolfson has combined functions from both of these domains in a single mixed-signal chip. The WM8350, the first product in the family, comprises an audio codec with a suite of regulators and dc/dc converters that will meet all of the power-management needs of a typical portable product, such as a mobile handset or media player. On the audio side, a high-fidelity audio codec has mixing capabilities, pop and click suppression, and signal/noise performance of 98 dB for its DAC at −84-dB THD (total harmonic distortion). The audio chain's ADC achieves SNR (signal-to-noise ratio) of 95 dB at −80 dB THD.

The chip has six analog inputs, two stereo analog outputs, and two monophonic line outputs; it also features on-chip headphone amplifiers that drive 20 mW into 16Ω with THD of −70 dB. Power-management functions switch and regulate multiple voltage lines. You can program four 2-MHz dc/dc step-down (buck) converters to provide 0.85 to 3.4V in 25-mV steps. The converters yield peak efficiency of more than 90%, and they need only a small external inductor and capacitor per line. To generate voltage above the battery line—for display backlighting and for the 5V necessary for USB—two 1-MHz boost converters also achieve more than 90% peak efficiency.

> Combining these mixed-signal functions on one chip can save 25% in external-component count and 50% in board area.

You can program four on-chip, 150-mA, low-noise, low-dropout regulators over 0.9 to 3.3V in 50- or 100-mV steps, depending on the version. To handle the lithium battery that typically powers the class of products that Wolfson has in mind for this chip, a single-cell charger—programmable for different cell voltages—has trickle and fast-charging modes. The charger finds its supply from USB or ac/dc source, as available, and allows product operation while charging an empty battery.

The chip has 13 I/O pins that you can use to control system functions: You can program, either at start-up or during operation, all of the outputs to set power-up and -down sequences using a dedicated onboard controller. The chip occupies a 129-pin, 7×7-mm BGA package with a 0.5-mm ball pitch. Wolfson acknowledges that, if you use all of the regulation functions at rated levels, the chip will dissipate 1 to 2W but says that you can use all of the lines together and stay within the chip's fully protected operating zone.

Combining these mixed-signal functions on one chip can save you 25% in external-component count and 50% in board area, the company says. The chip's designers synchronized audio and dc/dc-converter clocks to avoid on-chip-interference effects, but Wolfson claims that this step turned out to be largely unnecessary. Wolfson's expertise in physical and substrate phenomena on mixed-signal processes minimized unwanted effects.

—by Graham Prophet

▷**Wolfson Microelectronics**, www.wolfsonmicro.com.

DILBERT By Scott Adams

04.03.08

LCD CONTROLLER TACKLES HARSH ENVIRONMENTS

Digital View recently introduced the HE-1920 COTS (commercial-off-the-shelf) LCD controller. The fully buffered, multisynchronous interface controller provides analog and digital connections for a range of TFT (thin-film-transistor)-LCD panels with resolutions to 1920×1200 pixels. It features full-screen image expansion of lower resolutions, image-flip and -invert functions, and onscreen picture-in-picture functions.

The $269 (1000) HE-1920 also features a 16-bit bus connector that permits developers to create proprietary hardware interfaces for the controller. The interfaces provide software-managed selection pins to manage multiple input configurations, including optical inputs and additional ports. The ROHS-compliant HE-1920, targeting military and rugged industrial applications, features silicon-resin conformal coatings, an operating-temperature range of −40 to +80°C, and calculated MTBF greater than 100,000 hours.

—by Warren Webb

▷**Digital View, www.digitalview.com.**

The rugged HE-1920 COTS LCD controller supports high-resolution and high-definition formats in military or industrial applications.

Processor combines Coretex-A8 core with graphics and digital-signal processing

Texas Instruments' latest OMAP (Open Multimedia Applications Platform) processors integrate a superscalar, 600-MHz ARM (www.arm.com) Coretex-A8 core with DSP functions, HD (high-definition)-video acceleration, and 2- and 3-D graphics engines. The devices, which can operate with Windows CE or Linux operating systems, target applications with graphics interfaces and video capabilities for power-constrained products, such as handheld devices for home management and patient monitoring, as well as GUIs for consumer and home appliances.

The entry-level device of the family, the OMAP3503, is available for sampling and includes USB 2.0 HS (high-speed)-compliant OTG (On-The-Go) controllers with two additional USB-host controllers. It also includes a display subsystem with support for PIP (picture in picture), color-space conversion, rotation, and resizing. All the devices include interface support for LCDs, SDTVs (standard-definition televisions), and HDTVs (high-definition televisions) and support for LPDDR (low-power-double-data-rate), NOR, and NAND memories, along with SRAM and pseudoSRAM. The OMAP3503 is available for $19.95 (10,000) in a 0.4-mm-pitch package.

The OMAP3515 and 3530 add a 2- and 3-D graphics engine that supports Open GL ES (graphics language for embedded systems) 2.0 graphics based on Imagination Technologies' (www.imgtec.com) PowerVR SGX graphics accelerator that can deliver 10 million polygons/sec. The OMAP3530 adds a 64x+ DSP core and HD-video accelerators that can support performance to MPEG-4 SP with 720p decoding at 30 frames/sec. The OMPA3525 omits the Open GL ES 2.0 engine, but it includes the C64x+ DSP and HD-video accelerator of the OMAP3530 processor.

These processors use TI's SmartReflex technology, which allows the systems to dynamically control the voltage, frequency, and power consumption based on activity. The OMAP35x evaluation module includes an OMAP3503 processor with a Linux board-support package based on the 2.6.22 kernel, peripheral drivers, a U-boot for boot loading, and a Busybox-based root-file system. The $1499 evaluation module supports Ethernet, USB 2.0, SDIO (secure digital input/output), I²C, JTAG, keypad connectivity, and daughtercards. It sports S-video output via NTSC/PAL (National Television System Committee/phase-alternation-line) and YpbPr/RGB, and it can connect with CompactFlash, SD/MMC (secure-digital/multimedia-card), and DDR memories.

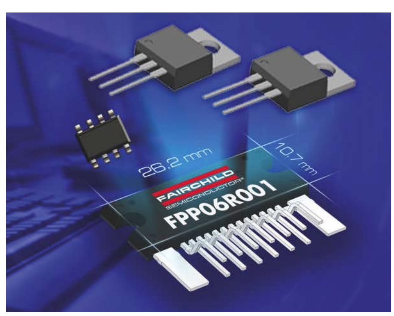
—by Robert Cravotta

▷**Texas Instruments**, www.ti.com.

MOSFETs get their 15 minutes of fame at APEC

One thing you can count on at the power-conversion industry's annual APEC (Applied Power Electronics Conference) is that MOSFETs will feature prominently. This year's conference, which took place last month in Austin, TX, was no exception, with new announcements from Infineon, Fairchild, and Toshiba, among others.

Infineon's 900V superjunction MOSFETs target high-efficiency SMPS (switched-mode-power-supply), industrial, and solar-energy applications. Infineon claims that the CoolMOS power-MOSFET family overcomes the "silicon limit," a characteristic of MOSFET semiconductors in which doubling of voltage blocking capability leads to a fivefold increase in on-resistance. In overcoming the silicon limit, the CoolMOS devices achieve the industry's lowest on-resistance per package type: 0.12Ω in a TO-247 package, 0.34Ω in a TO-220 package, and 1.2Ω in a D-Pak. The company claims that these figures are at least 75% lower than those for conventional 900V MOSFETs. The volume price for a 120-mΩ part in a TO-247 package is less than $3.50.



Fairchild's Power-SPM FPP06R001 synchronous-rectifier module offers 10% lower on-resistance and 16% less stray inductance than comparable discrete designs.

Using discrete MOSFETs on a board can increase manufacturing costs and resistance between parts. Fairchild attacks this problem by incorporating two PowerTrench MOSFETs and a high-current gate driver into its EPM15-packaged Power-SPM FPP06R001, which replaces as many as 10 discrete components. Fairchild claims the advanced package accounts for 10% lower on-resistance and 16% lower stray inductance than comparable discrete approaches. The devices cost $5.

Toshiba announced a family of high-speed switching MOSFETs, which the company based on its UMOS VI-H sixth-generation trench process. The new devices enable increased power efficiency by lowering on-resistance and increasing switching speed through lower gate charge and lower gate resistance. The new MOSFETs also feature aluminum-strap connections instead of conventional wire-bond technology to further reduce on-resistance. The devices will find use as low-side MOSFETs in dc/dc-converter applications. Features include a maximum drain-to-source voltage of 30V, a maximum drain current of 50A, and a typical on-resistance of 2 mΩ. Packaging options include a low-profile SOP Advance measuring 5×6×0.95 mm. Prices start at 65 cents.

—by Margery Conner

▷**Applied Power Electronics Conference**, www.apec-conf.org.
▷**Fairchild**, www.fairchildsemi.com.
▷**Infineon**, www.infineon.com.
▷**Texas Instruments**, www.ti.com.
▷**Toshiba**, www.toshiba.com.

1-μHz to 240-MHz generator produces precision pulses, 14-bit arbitrary waveforms, and more

Design and test engineers are under increasing pressure to quickly bring high-quality products to market and differentiate those products from their competition. Achieving these objectives requires new test protocols and new classes of instruments, says Alois Hauk, vice president and general manager of digital-photonic test at Agilent Technologies, which has introduced what the company calls the industry's first generator to combine superior signal quality with the ability to produce such a wide variety of waveforms over such a broad frequency range.

The 81150A pulse/function/arbitrary-waveform/noise generator employs a 512k-sample/channel arbitrary-waveform memory and a 14-bit DAC that operates as fast as 2G samples/sec. The generator can produce signals with repetition rates as low as 1 μHz with modulation at frequencies as high as 10 MHz.

The unit, which produces many waveforms greater than 100 MHz and sine waves to 240 MHz, suits use in general-purpose bench tests and advanced serial-data stress tests.

The 81150A provides versatile generation of pulses with tight control over transition times and other parameters; standard, arbitrary, and modulated waveforms; and noise for stress testing. The generator works well with the manufacturer's 5/6/80000 Infiniium real-time oscilloscopes and DCA-J sampling oscilloscope for serial-data testing. Integration of many functions into one instrument minimizes cabling, space, and test-setup time.

Engineers must create ideal and worst-case signals to obtain rapid, accurate insights into designs for such devices as semiconductor circuits, sensors, and modulators. The 81150A's accurate signals help engineers to test their devices—not the signal source.

With 14-bit resolution and outputs from 1 μHz for a variety of signals to 240 MHz for sine waves, the compact 81150A may provide all of the capabilities you need for generating precision pulses, functions, arbitrary waveforms, and noise to well beyond 100 MHz.

"When signal fidelity matters, 'just enough' signal quality isn't enough," says Hauk. "Versatile waveforms and the most precise signals are key contributors to developing quality products within a reduced design cycle. The pulse/function/arbitrary-waveform/noise generator supports engineers through each development phase, and the patented noise generator enables a quantum leap in productivity."

The instrument provides both "random" and calibrated, deterministic noise for repeatable stress tests. (The random noise is not truly random, but you can set the signals to repeat as infrequently as every six to 12 hours; you can also choose much more frequent repetition.) You can define various stress tests simply by adjusting the crest factor, a measure of signal quality equal to the ratio of peak or peak-to-peak-to-rms voltages.

The 81150A features accurate signals that test the device—not the source—with intrinsic jitter of 8-psec rms at any frequency and has 13 standard functions, modulation capabilities to 10 MHz, and more than 80 measurement types. It also has differential output and high-voltage output amplifiers to test state-of-the-art devices. The 81150A is available in one- and two-channel versions; prices start at $8900.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/81150.

FAST SPICE SIMULATOR TARGETS DIGITAL, MIXED-SIGNAL, AND ANALOG DESIGNS

04.03.08

EDA start-up Nascentric Inc has introduced a Fast Spice simulation tool for analog, mixed-signal, and custom digital designs that claims true Spice accuracy and higher speeds than other commercial Fast Spice simulators.

The OmegaSim tool uses a patented current-based SPICE model and engine. It quickly classifies elements in a design, groups them, and then assigns each group to a simulation engine that the company optimized for a particular operation. "Each of the engines focuses on what it does best," says Rahm Shastry, Nascentric's president and chief executive officer. "The transistor engine is complex, but you don't need the same complexity for interconnect because interconnect is only RLC [resistance/inductance/capacitance]. Thus, the interconnect engine can be much simpler, and interconnect can simulate fast and accurately. The same goes for SRAM-bit cells, which go to an SRAM engine."

OmegaSim also has multithreaded engines, further speeding simulation. Users can run the tool in digital or analog mode. The digital mode has a submode for verification or analysis. In digital mode operating on one thread, the tool typically runs 10 times faster than other commercial Fast Spice simulators, Shastry claims.

On a multithread platform, such as an Intel (www.intel.com) CoreDuo, the tool can run two times faster. In digital-verification mode, the tool provides 2 to 4% the accuracy of Spice, and, in digital-analysis mode, the tool provides 1 to 2% the accuracy of Spice.

Nascentric licenses the tools under a thread-based licensing model. It costs $1200/thread/month or $12,000/thread/year for the digital-only version. The company offers the mixed-signal tool for $500 more per thread/month or $5000 more per thread/year.

—by Michael Santarini

▶**Nascentric, www.nascentric.com.**

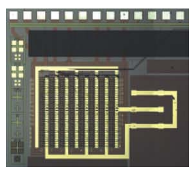
RESEARCH UPDATE

BY RON WILSON

Stanford tries nanotubes for on-chip interconnect

A recent paper in *Nano Letters* illustrates both why researchers are so interested in carbon nanotubes as an interconnect medium and why making the nanomaterials a useful reality is such a hurdle. Researchers at Stanford University, working with support from Toshiba (www.toshiba.com) and foundry services from TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com), have successfully connected ring oscillators using nanotubes from a commercial third party. The hit-or-miss results displayed oscillator frequencies as high as 1 GHz—a first for this new material.

TSMC fabricated a die with 256 ring oscillators; one interconnect link was missing from each ring. The Stanford/Toshiba team then attempted to make this one missing connection using commercially manufactured metallic-mode nanotubes. They succeeded for 19 of the 256 circuits. Of those 19, 16 of the connections showed impedance low enough to allow the oscillators to operate at frequencies greater than 800 MHz, and one achieved 1.02 GHz. The team used nanotubes measuring 50 to 100 nm in diameter and approximately 5 microns long. HS Phillip Wong, professor of electrical engineering at Stanford and co-author of the paper, observes that significant improvements in both the quality of the nanotube stock and the technology of connecting the tubes to transistor contacts would be necessary before the technique approached production viability. But the experiment shows that the nanotubes can at least achieve reasonable frequencies.



Carbon nanotubes form connections in ring oscillators in this research die.

▷**Stanford University**, www.stanford.edu.

FEEDBACK LOOP

"There is no one that I trust less to make intelligent economic or engineering decisions than Congress, which, through previous idiotic legislation, is one of the primary contributors to high energy prices by making it nearly impossible to develop new, economically viable sources of energy.

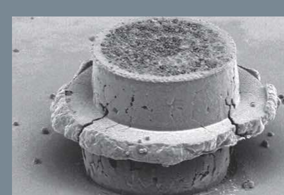
—Reader Herm Harrison, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6531582.

GEORGIA TECH STUDIES OFF-CHIP-INTERCONNECT ISSUES

As chips get faster, off-chip interconnect increasingly looks like a bottleneck to high-frequency signals. This scenario occurs when the signals must traverse not only relatively long distances across a board, but also short hops from the package leads to the board traces. A pair of studies at the Georgia Institute of Technology School of Chemical and Biomolecular Engineering is exploring these challenges.

In the first study, researchers attempted to fabricate an all-copper structure to bond package-lead frames to PCBs (printed-circuit boards), reasoning that such connections should be lower in series resistance than the traditional flow-soldered-bump technology. The team electroplated copper bumps onto both the package pads and the PCB pads. Then, placing the package on the board and aligning the bumps, they immersed the assembly in an aqueous-copper solution, allowing a thin pillar of metallic copper to grow between the bumps.

The result is too thin to be structurally adequate in that state, so the team then annealed the assembly at 180°C for one hour—not necessarily the most welcome step for process engineers but enough to strengthen the copper pillars. The result is a strong, low-resistance connection.



Two copper pillars bond together using a novel fabrication technique. Placing these all-copper connections between computer chips and external circuitry will lead to increased computing speeds (courtesy Tyler Osborn).

For board-crossing, the second study experimented with forming conductors with buried air gaps beneath them to reduce parasitic capacitance. The process involves plating copper traces onto an epoxy-fiberglass board and then coating the traces with a layer of sacrificial polymer. A layer of a different polymer then builds up around the traces. A titanium barrier and a top copper layer go over the original traces on top of the sacrificial polymer. The scientists then cook away this sacrificial polymer at 180°C. The result is a multilayer connection of copper, air gap, titanium, and copper.

The team has demonstrated formation of this structure and is working on a version that would in effect form a coaxial cable.

▶**Georgia Institute of Technology, www.gatech.edu.**

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32 Kb	25AA320A	25LC320A	
16 Kb	25AA160A/B	25LC160A/B	
8 Kb	25AA080A/B	25LC080A/B	
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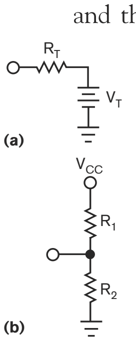
BY HOWARD JOHNSON, PhD

Designing a split termination

My last two articles dealt with the design of the end-terminating structure in **Figure 1a** (**references 1** and **2**). That structure terminates a transmission line with a single resistor value, R_T (termination resistance), leading to a fixed V_T (terminating voltage). In most cases, the termination resistance equals the characteristic impedance of the transmission line or can be a little higher than that impedance if the driver is weak. The ideal terminating voltage centers the digital waveform, producing equal voltage margins above and below the required switching levels, V_{OH} (high output voltage) and V_{OL} (low output voltage). That ideal voltage equals the average of the required high- and low-output levels minus a correction term that accounts for asymmetry in the drive capability of the source:

$$V_T = \frac{V_{OH}+V_{OL}}{2} - R_T\frac{I_{OH}+I_{OL}}{2}.$$

This **equation** assumes that the I_{OH} (high-side source current) is positive and the I_{OL} (sinking current) is negative. If those two values have equal magnitudes, they sum to zero.



$$\frac{1}{\frac{1}{R_{TMIN}} - \frac{1}{R_{2MIN}}} < R_1 < \frac{1}{\frac{1}{R_{TMAX}} - \frac{1}{R_{2MA}}}$$

$$\frac{V_{CCMAX}-V_{OL}}{\frac{V_{OL}}{R_{2MAX}} - I_{OL}} < R_1 < \frac{V_{CCMIN}-V_{OH}}{\frac{V_{OH}}{R_{2MIN}} - I_{OH}}.$$

Figure 1 If R_1 meets both the termination-impedance constraints (a) and the drive-current constraints (b), then both termination circuits perform equally well.

If you have a suitable source of terminating voltage, the structure in **Figure 1a** is easy to understand and uses fewer components than the one in **Figure 1b**. On the other hand, if no suitable voltage source exists, then you have no choice: You must synthesize the Thevenin equivalent from **Figure 1b**.

Given any combination of termination resistance, termination voltage, and V_{CC} (power-supply voltage) with voltage greater than the termination voltage, the following circuit values make the circuit in **Figure 1b** perform, from the transmission line's perspective, just as well as the one in **Figure 1a**.

$$R_2 = R_T\frac{V_{CC}}{V_{CC}-V_T}; \qquad R_1 = R_T\frac{V_{CC}}{V_T}.$$

If you carefully follow the **equations**, you are now almost finished with your design. Next, you will discover that, no matter what values you have just computed, those exact values are never available in your component catalog. The values in the catalog are quantized to the nearest standard value, according to the tolerance specification for each component.

If you want your circuit to perform over a range of resistor values and over a range of possible values for the power-supply voltage, check the worst-case constraints in **Figure 1**. If resistor R_1 meets these conditions, then the circuit in **Figure 1b** will work under all conditions just as well as the one in **Figure 1a**. Make sure that the minimum and maximum values take into account temperature and aging. Some fiddling with the values will be necessary; there is no straightforward design approach that always works.

If you have difficulty satisfying the constraints, try raising your target for the termination resistance and start again. Although it will not terminate the circuit as well, increasing the termination resistance opens more room for tolerance in the circuit. The tolerance requirements for R_1 and R_2 are somewhat interchangeable. A tighter tolerance for R_2 opens more room for R_1 and vice versa.

I cannot help you further with this aspect of the design. Component selection in analog circuits always involves some last-minute juggling to meet all the tolerance requirements. I can, however, point out that the circuit in **Figure 1a** helps you understand the need for two resistor values and how they work together to meet the impedance and current-drive constraints your driver imposes. **EDN**

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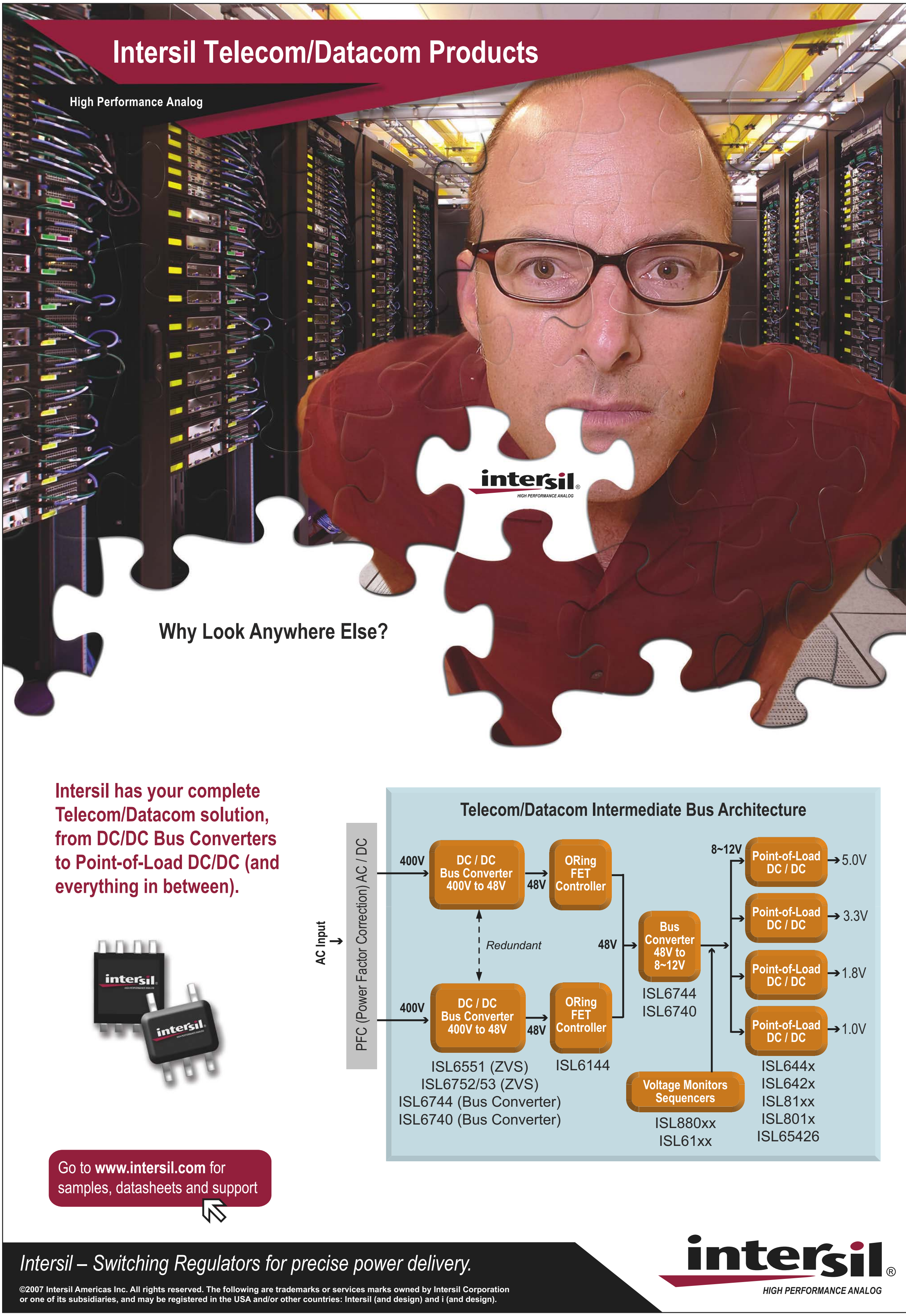
Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.



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48V
ORing FET Controller
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ISL6752/53 (ZVS)
ISL6744 (Bus Converter)
ISL6740 (Bus Converter)
ISL6144
48V
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HIGH PERFORMANCE ANALOG

BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Honest energy

I had the honor and great pleasure of serving as a panelist at an APEC (Applied Power Electronics Conference, www.apec-conf.org) rap session in February in Austin, TX. Although the session's central theme was the power sector's focus on efficiency, I was intrigued to note that all of the panelists agreed on an issue concerning energy use that lies outside a strict definition of efficiency: watts out divided by watts in.

As typical household products become more sophisticated, the power factor of the load they represent decays—a trend that is exacerbating a growing stress on our electric-power infrastructure. The problem with low power-factor loads is that they tie up grid capacity in excess of the energy they use.

An analysis of a load that draws nonsinusoidal current represents the current waveform as a harmonic series with components that are either in phase or in quadrature with the voltage waveform. Because the power grid must supply all of the current—the in-phase component, which the utility meter measures, and the out-of-phase or reactive component, which the utility meter does not measure—the grid load exceeds the metered load.

The so-called P_A (apparent power) is the product of the rms voltage and rms current—measures that ignore relative phase (**Figure 1**). P_{REAL} (real power) is the integral of the in-phase voltage-current product over each line cycle. P_{REAC} (reactive power) accounts for the quadrature-current component. The PF (power factor) is a measure of grid-use efficiency, which you can calculate as the ratio of P_{REAL} to P_A, or

$$\frac{P_{REAL}}{\sqrt{P^2_{REAL}+P^2_{REAC}}}.$$

Conversely, the excess grid capacity that a load uses is

$$\frac{P_A-P_{REAL}}{P_{REAL}}=\frac{1}{PF}-1.$$

The **figure** shows a load with a PF of about 0.9, which corresponds to an excess grid use of about 12%. To put numbers to a few real objects, I measured some devices in my home (**Table 1**). Think of these numbers in the context of the electronic devices your company makes and consider the important role high power factors can play in electric-energy availability.EDN

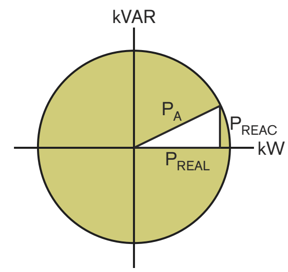

Figure 1 Power factor is the ratio of real-to-apparent power and is a measure of grid-use efficiency.

TABLE 1 POWER FACTORS, EXCESS GRID USE

Device	Power factor	Excess grid use (%)
Home computer	0.65	54
Computer-CRT display	0.65	54
Laser printer	0.73	37
Compact fluorescent lamp	0.56	79
Tungsten-filament lamp	1	0
Refrigerator compressor	0.91	10

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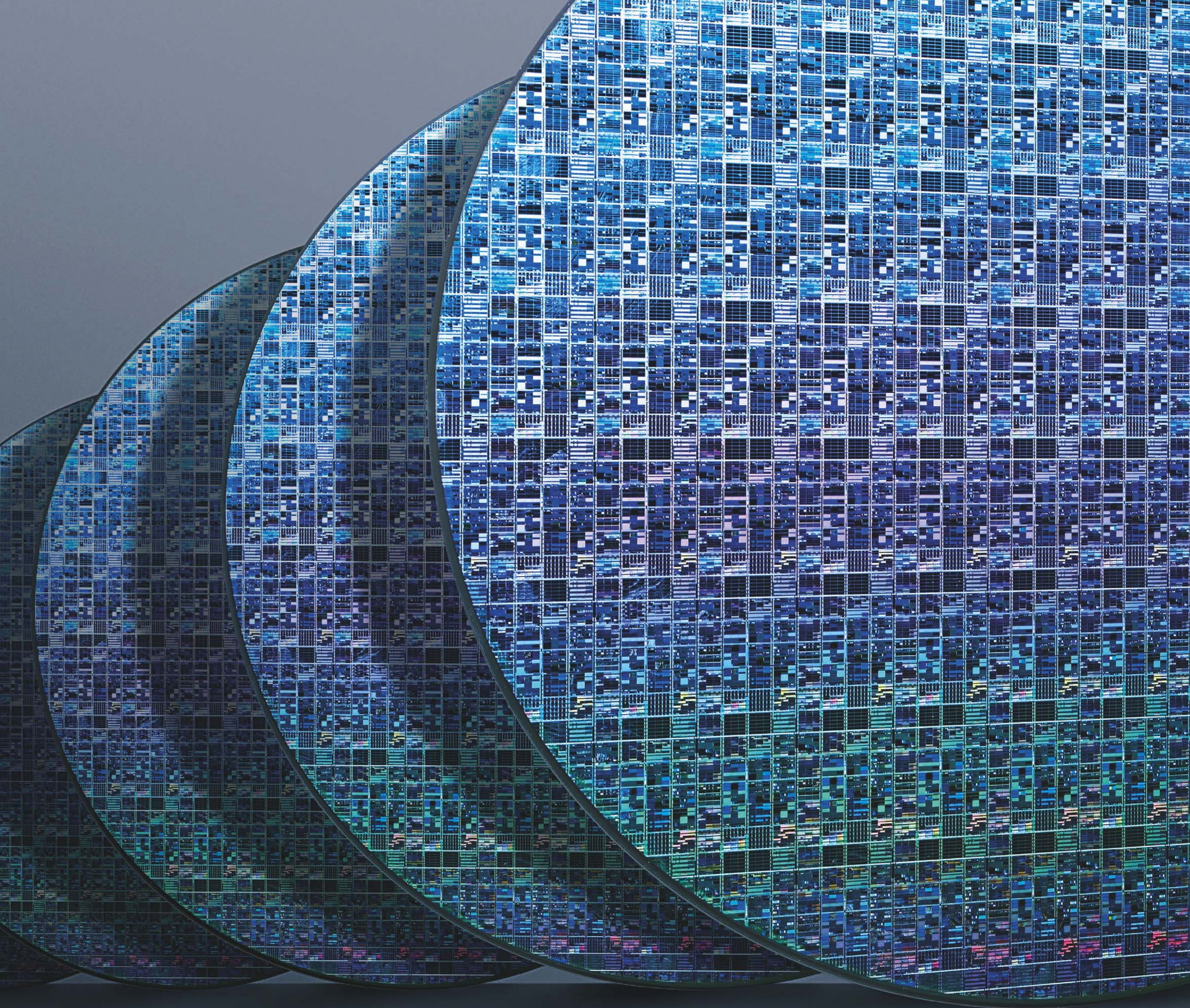

Analog Applications Journal

DESIGN BRIEF

Using a Buck Converter in an Inverting Buck-Boost Topology

By John Tucker
Applications Engineer

Introduction

To power some applications, generating a negative voltage from a positive input voltage source may be required. In such instances it is possible to configure the buck converter into an inverting buck-boost topology, where the output voltage is negative with respect to ground.

Basic Buck Topology

To understand the inverting buck-boost circuit operation, first consider the basic topology of the buck converter as shown in Figure 1. The components inside the box with a blue dotted outline are typically integrated into the converter's integrated circuit, while those outside are required external components.

When the FET switch is on, the voltage across the inductor is $V_{IN} - V_{OUT}$, and the current through the inductor increases at a rate of

$$\frac{di}{dt} = \frac{V_{IN} - V_{OUT}}{L}.$$

When the switch is off, the inductor voltage reverses to keep the inductor current continuous. Assuming that the voltage drop across the diode is small, the inductor current ramps down at a rate of di/dt = V_{OUT}/L. The steady-state load current is always carried by the inductor during both the on and off times of the FET switch. The average inductor current is equal to the load current, and the peak-to-peak inductor ripple current is

$$I_{L(PP)} = \frac{(V_{IN} - V_{OUT})\,D}{f_{SW} L},$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, D is the duty cycle V_{OUT}/V_{IN}, f_{SW} is the switching frequency, and L is the output inductance.

Inverting Buck-Boost Topology

Compare the preceding operation to that of the inverting buck-boost topology shown in Figure 2. The inductor and catch diode have switched places relative to the buck converter of Figure 1; and the output capacitor is reversed in polarity, as the

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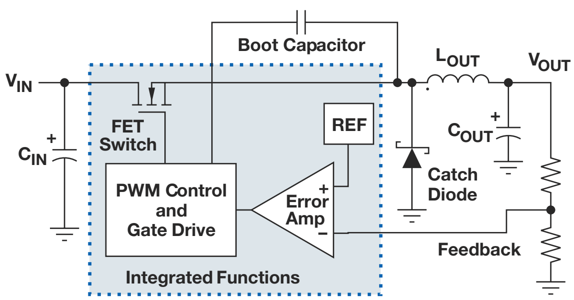

Figure 1. Buck topology

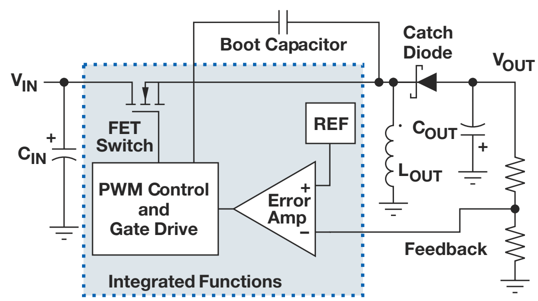

Figure 2. Inverting buck-boost topology

TEXAS INSTRUMENTS

output voltage is negative. During operation, when the FET switch is on, the voltage across the inductor is V_{IN} and the current ramps up at a rate of $di/dt = V_{IN}/L$. While the FET switch is on, the entire load current is supplied by energy stored in the output capacitor. When the FET switch turns off, the inductor reverses polarity to keep the inductor current continuous. The voltage across the inductor is approximately V_{OUT}, and the inductor current decreases at a rate of $di/dt = –V_{OUT}/L$. During the off time, the inductor supplies current both to the load and to replenish the energy lost by the capacitor during the on time. So for the buck-boost circuit, the average inductor current is

$$I_L = \frac{I_{OUT}}{1-D},$$

and the peak-to-peak inductor current is

$$I_{L\,(PP)} = \frac{V_{IN} D}{f_{SW} L}.$$

The duty cycle, D, is approximately

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}}.$$

These basic differences in circuit operation are important when the buck converter is used as a buck-boost converter.

Design Considerations

When a nonsynchronous buck converter is used in an inverting buck-boost configuration, certain considerations must be made. The design equations are presented in simplified form with the semiconductors idealized and other component losses neglected. To implement the buck-boost topology of Figure 2, the buck-converter ground pin is connected to V_{OUT}, and the positive lead of the output capacitor is connected to ground. The voltage across the device's V_{IN} pin to GND is then $V_{IN} – (–V_{OUT})$, rather than just V_{IN} as in the buck converter. This combined voltage must be less than the specified V_{IN} of the chosen device.

Since the average output current cannot exceed the device's rated output, the available load current is reduced by a factor of 1 – D. So for this design, the maximum available DC load current is $I_{SW} \times (1 – D) = I_{Load}$, where I_{SW} is the average rated current of the high-side switch FET.

Typical Waveforms

To demonstrate some of the performance characteristics of an inverting buck-boost converter, a test circuit was constructed. The circuit used a 24-V input and had a –5-V output at 2 A. Output voltage ripple and switching-node waveforms are shown in Figure 3. Note that the switching-node voltage varies from V_{IN} to V_{OUT} for the inverting buck-boost converter instead of V_{IN} to ground for a buck converter. The

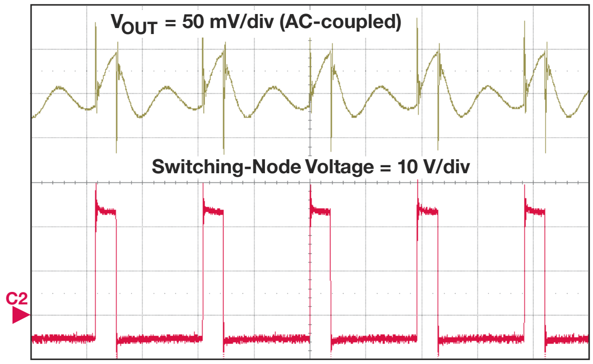

Figure 3. Inverting buck-boost output voltage ripple and switching-node voltage

ground reference line is indicated by the C2 marker at the left edge of the figure. Also observe that the output voltage ripple does not show the linear ramp characteristic typical of the buck converter. The output capacitor supplies the load current during the switch on time and is recharged during the switch off time. This charge-and-discharge cycle is superimposed with the AC ripple current to create a more complex ripple current as shown in the figure. Remember that the output voltage is negative, so the positive portions of the waveform represent the output becoming less negative, or the discharge portion of the cycle.

Conclusion

A buck converter can be used to generate a negative output voltage from a positive input voltage if the circuit is configured as an inverting buck-boost converter. The circuit design is straightforward, but these important points should be remembered. The output current is less than the average inductor current by a factor of 1 – D, so the available output current will be less than the device rating. The output voltage is negative and is available at the device ground pin, so the effective voltage across the input of the device is $V_{IN} – V_{OUT}$. This difference must not exceed the input-voltage rating of the device. Finally, the ground of the device should not be tied to the system ground.

Please see Reference 1 for the complete version of this article, which provides additional design details and shows waveform comparisons between test circuits for a buck converter and the inverting buck-boost converter.

Reference

1. View the complete article at http://www-s.ti.com/sc/techlit/slyt286

BASE STATIONS AND HANDSETS NEED RF AMPLIFIERS WITH HIGH LINEARITY AND EFFICIENCY. WITH SOME CLEVER TECHNIQUES, DESIGNERS CAN ALIGN THESE MUTUALLY EXCLUSIVE GOALS.

Heads and ~~or~~ tails

BY PAUL RAKO • TECHNICAL EDITOR

DESIGN RF AMPLIFIERS FOR LINEARITY AND EFFICIENCY

Cell phones use modern modulation schemes that require linear amplification of the RF signal. A typical way to achieve this linearity is to burn more power in the output stage. This approach reduces efficiency, even though efficiency is one of the most important operating parameters in a phone, a base station, or any other electronic system.

Important efficiency requirements exist on both the handset and the base-station sides of the telecom world. In handsets, efficiency directly translates into battery life. By increasing cell-phone efficiency, you can also increase talk time—a fundamental figure of merit for a handset. On the base-station side, efficiency results in lower electric bills and, just as important, less heat. Reducing heat and power consumption creates a cascading set of results that provide lower initial costs, lower operation costs, and lower total cost of ownership.

In older cell-phone-modulation designs, the linearity of the output stage was unimportant because the demodulation did not depend on linearity. CW (continuous-wave), FM (frequency-modulation), and GMSK (gaussian minimum-shift keying) for GSM (global-system-for-mobile) communication technologies have a constant envelope and require no linear amplification. To work properly, new modulation schemes, such as EDGE (enhanced data for GSM evolution), require linear amplifiers. You can achieve this linearity by underdriving the RF amplifier and leaving head room between the output signal and the power-supply voltage. The problem with this approach is that it directly decreases the amplifier's efficiency.

Efficiency in single-transistor output stages improves as the output swing approaches the power-supply rails. To improve efficiency, select power-supply voltages and load impedances so that the output stage swings close to the rails. This approach dissipates less average power in the output transistors because the output transistor always has less voltage across it as the output signal nears the power rail.

Unfortunately, driving the output signal closer to the supply rail also reduces the amplifier's linearity. This reduction occurs just as frequently at RF frequencies as it does at audio frequencies. Any amplifier whose circuit design causes it to swing to values near the power-supply rails has less linearity. The ultimate expression of linearity problems in an amplifier is amplifier clipping, and the power-supply voltage is insufficient to allow the signal excursion to properly represent the amplified input signal (**Figure 1**).

THE NEED FOR LINEARITY

It may not be immediately apparent, but linearity is not a primary concern in designing many RF systems. The fact that designers use Class C amplifiers should suggest that a perfect representation of the input sine wave might not be critical to the communications requirements of some types of signals. Imagine the RF signal from an FM-radio station. In FM transmissions, the zero crossings of the waveform contain all the information in the signal. Even if the peaks of the waveform become distorted, the fidelity of the demodulated signal do not. Overdriven FM-radio signals create frequency harmonics of the carrier frequency, and those harmonics may be objectionable from an interference standpoint, but a receiver tuned to an overdriven-FM-radio signal still operates successfully (**Figure 2**).

Over the past decade, the acquisition costs and revenue demands of cell-phone-radio bands have encouraged the design of advanced modulation schemes that allow for more information in a narrower frequency band. A figure of merit for these schemes is bandwidth efficiency, which you express in megabits per megahertz or bits per second per hertz. Modern and proposed cell-phone standards, such as EDGE, contain information in far more than the zero crossings of the signal. The new cell-phone-modulation schemes, such as QAM (quadrature-amplitude modulation), carry information in both the phase and the amplitude of the envelope signal on the RF-carrier frequency. Examine the classic 64-QAM (64-state-QAM)-vector constellation (**Figure 3**). The phase and amplitude of the signal use a series of symbol vectors to create the envelope of the RF signal. Because there are 64 vectors, the information that any vector carries can represent 6 bits of digital information, providing the bandwidth efficiency of 64-QAM schemes, which approach 6 Mbps/MHz.

AT A GLANCE

- New cell-phone standards require linear RF amplifiers.
- Improving linearity often hinders efficiency.
- Digital predistortion is one method of achieving linearity and efficiency.
- The Doherty amplifier implements a hardware method for improving efficiency.
- Modeling and simulating nonlinear systems are challenges.

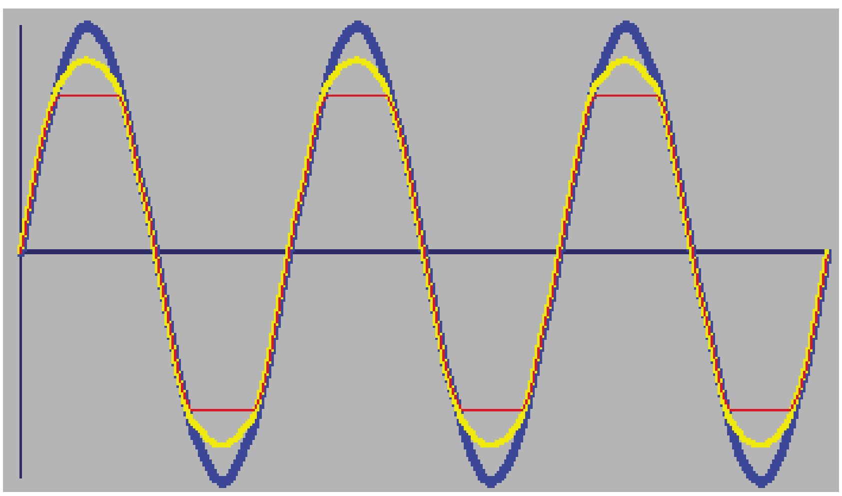

Figure 1 Clipping distortion is apparent when comparing the blue input with the yellow, moderately clipped output waveform or the red, heavily clipped output waveform. Symmetrical clipping such as this one appears as odd harmonics in the frequency domain. Amplifier nonlinearity creates intermodulation distortion that is harmonically unrelated to the two input tones.

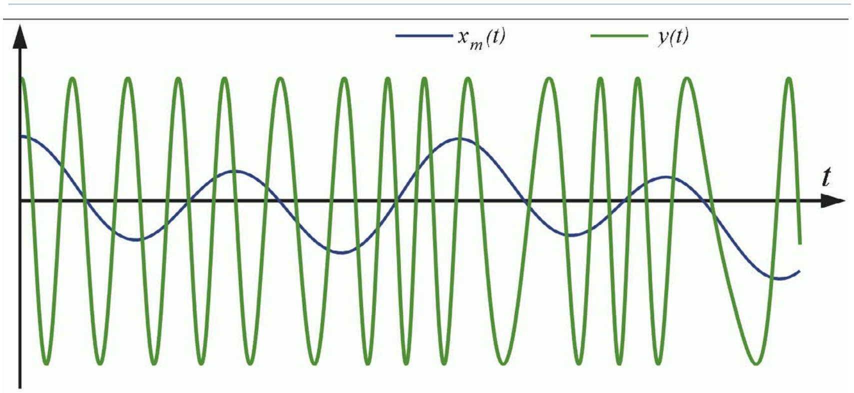

Figure 2 The frequency-modulated signal, y(t), is immune to amplifier nonlinearity. The zero crossings, rather than the amplitude, contain the information, so amplitude distortion in the amplifier causes no problems.

Poor linearity causes problems in such an advanced modulation scheme. Because the demodulator needs an accurate depiction of both the amplitude and the phase of the signal, the instantaneous accuracy of the signal is important, unlike with FM transmissions, in which only the zero crossings matter. If the operating signals drive the RF-power amplifier close to the output rail, the transistor approaches saturation, compounding its inherent logarithmic nonlinearity. Thus, the symbol vector that the amplifier encodes loses the correct amplitude and phase. When the nonlinearity is severe enough, the symbols overlap and lose the information.

A demodulation scheme might account for the inherent nonlinearity of a transistor, but the biasing of that transistor establishes at which point on the logarithmic-transfer function the transistor operates. Thus, coming up with such a demodulation scheme would be difficult. Further, the saturation of the transistor as it approaches the power rails would be difficult to factor into to any demodulation scheme because each RF source has a somewhat arbitrary power-supply voltage. The only approach to correcting poor symbol accuracy is improving the accuracy of the RF-power amplifier.

Class A output stages have inherent nonlinearity due to the transistor's curve, making the positive and the negative excursions of the output sig-

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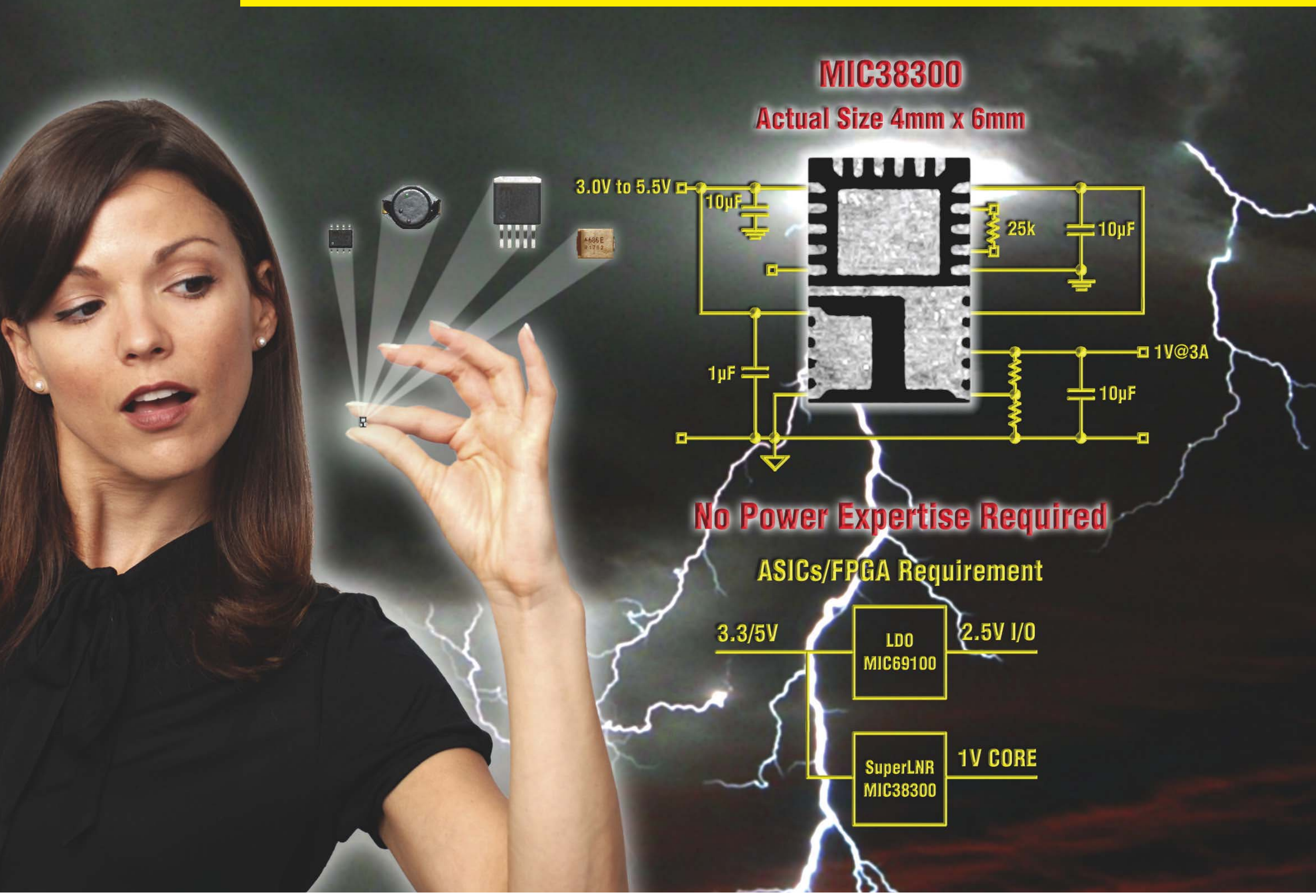

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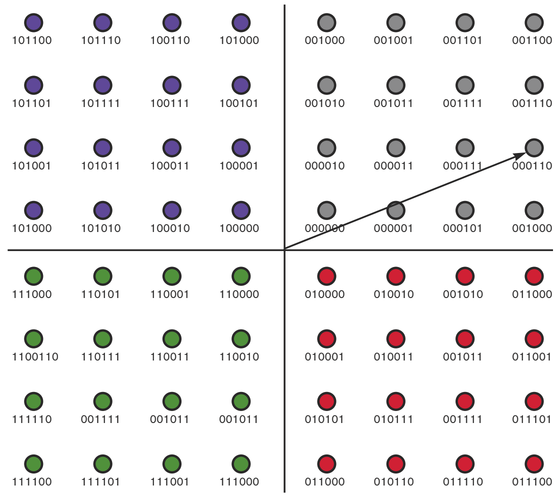

Figure 3 A 64-QAM constellation can encode 6 bits per symbol vector. Some vectors are subject to phase errors, and some vectors are sensitive to amplitude errors. In either case, the accuracy of the waveform envelope is critical, which makes amplifier linearity so important.

nal asymmetrical. At lower frequencies, feedback overcomes this nonlinearity. Transistor amplifiers soon evolved into operational amplifiers that have forward gain that can exceed 120 dB, enabling designers to improve linearity by using a large amount of negative feedback. This feedback combines with Class A-B output stages to produce linearity such as that of the National Semiconductor LME49710, which specifies a linearity of 0.00003%. Note, however, that this linearity spec is for operation at relatively low frequencies. All amplifiers exhibit a roll-off of gain with frequency. Current-feedback-amplifier architectures have less gain loss at high frequencies, but they still roll off at high frequencies.

Remember that the linearity improvement you achieve with large feedback involves also having a large forward gain. Because amplifiers have less forward gain at higher frequencies, they also have less feedback at high frequencies. As a result, RF amplifiers, especially RF power amplifiers, cannot use conventional feedback at the 1-GHz and higher frequencies at which they operate.

Just as daunting, the open-loop nature of most RF amplifiers means that they are subject to power-supply-rejection and output-saturation problems. Because RF amps operate near the frequency limits of the transistors themselves, you cannot practically make them into high-gain operational amplifiers. In this regard, RF-amplifier design still incurs all the difficulties that designers of tube equipment faced decades ago.

In addition to the linearity problems facing all amplifier designers, other linearity impediments make RF amplifiers even more challenging. For example, the electrical and thermal operation of the amplifier can cause memory effects that in turn introduce time- or data-dependent nonlinearity. Electrical-memory effects are analogous to the memory effects that you can observe in old tube-guitar amplifiers. These amps had cheap power-supply systems—often, open-loop linear supplies comprising a capacitor hanging across a tube-rectified line voltage. A loud power chord would heavily drive the output stage and pull down the power-supply voltage as the capacitor drained. The line voltage restores the capacitor after the heavy load, but it takes 10s of milliseconds to do so. The sag in the power-supply voltage changes the biasing of the output transistors in the guitar amplifier, creating distinct "data-dependent" nonlinearity. The degree of nonlinearity depends on the previous signal. RF-power amplifiers are subject to the same phenomenon. The sequence of data may require symbols that cause the heavy driving of the amplifier. This situation affects the power supply and biasing of the amplifier and creates time-dependent nonlinearity that changes with the modulation of the RF carrier.

Besides these electrical-memory effects, amplifier designers must also handle thermal-memory effects. Hot and cold transistors have different transfer functions, introducing a time-dependent nonlinearity into the system. If the environment is hot or the data stream heats up the output stage, then the transistor exhibits different nonlinearity from what it would exhibit at a cool temperature. As more CMOS chips are integrating RF-power amplifiers, even more thermal problems emerge.

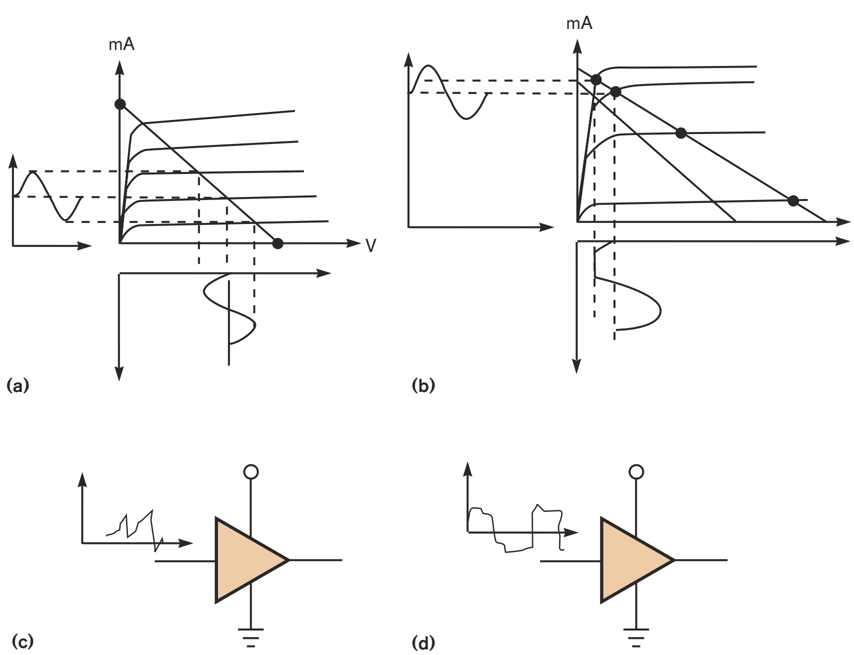

Figure 4 RF-power-amplifier nonlinearity occurs because of the inherent nonlinearity of a transistor amplifier (a), clipping distortion (b), and both electrical-memory (c) and thermal-memory (d) effects.

Figure 4 shows the nonlinearity of RF-power stages. At the core of transistor nonlinearity is the fact that the current-to-voltage transfer function of a

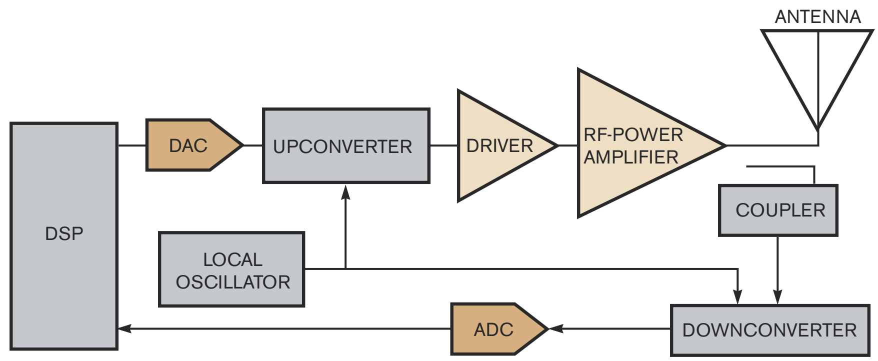

Figure 5 A cell-phone base station uses digital predistortion depending on the components the base station uses. Cartesian feedback also allows dynamic algorithms that can help compensate for memory effects and other nonlinearity.

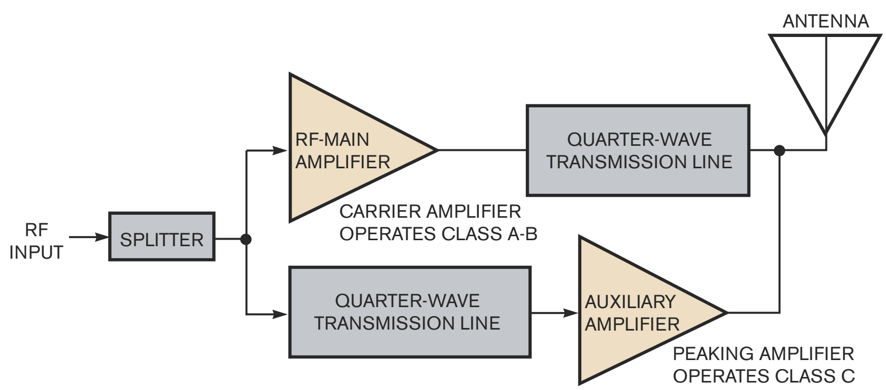

Figure 6 The Doherty RF amplifier achieves better efficiency by using an auxiliary amplifier to vary the load impedance on the primary amplifier. This approach allows the primary amplifier to continue to swing a large signal, dissipating less power in the amplifier. If the auxiliary amp lowers the load impedance on the primary amplifier, the primary amplifier delivers more power.

transistor is a logarithmic curve, not a straight line. The next issue is the saturation of the transistor as it approaches the power-supply rail.

APPROACHES TO LINEARITY

RF designers cannot just swing the output of the amplifier across a smaller range and suffer with the efficiency hit. They can use feedback, feedforward, or predistortion approaches to preserve efficiency for battery life and power savings. The feedback approach suits designs requiring high linearity, narrow bandwidth, and medium efficiency. The feedforward technique also works for designs requiring high linearity but with wide bandwidth and a low-efficiency requirement. Predistortion allows for medium linearity and bandwidth but yields high efficiency. Because RF-power amplifiers operate at such high frequencies, the use of conventional feedback techniques is impractical. In this context, the term "feedback" often refers to Cartesian feedback, in which circuitry converts the RF output back down to baseband, deriving the I (in-phase) and Q (quadrature) signals and feeding those signals back to the input stages. This system can achieve high linearity but only if you don't overdrive the output stage. The efficiency is lower than you might think. Because feedback amplifiers are subject to oscillation, you cannot use this technique on wideband amplifiers.

To get both acceptable linearity and high bandwidth, RF designers have resorted to predistortion techniques: The I and the Q signals that perform the modulation can compensate for the deterministic nonlinearity of a system. Because a digital system can also use complex algorithms to predict the thermal- and electrical-memory effects, these setups also preserve linearity in the face of these problems. Note that the inherent linearity of the components in the RF-signal path is still relevant. There is a limit to the corrections that you can apply in the digital domain. The closer the signal path is to ideal, the easier job a digital-system designer will have providing an accurate predistorted signal.

Designers are always cognizant of the inherent linearity of system components, according to James Wong, high-frequency-product-marketing manger at Linear Technology. "An active upconverter with built-in amplification, noise, linearity, and superior isolation results in a superior dynamic range … compared with a passive upconverter followed by an amplifier," he says. "This [approach] greatly reduces the challenge [for] digital designers … providing predistortion to the signals." He points out that modern base stations also use Cartesian feedback. Circuitry downconverts and extracts the I and Q components of the output and then feeds them back to the DSP core. This approach allows the system to use sophisticated algorithms that use real-time Cartesian feedback as well as predistortion based on the components the signal chain uses (**Figure 5**).

Hardware designers need not resort to using digital predistortion to improve linearity, however. Hardware can also improve linearity and efficiency; the better the inherent linearity, the less digital systems must correct. Designers may want to consider the use of a Doherty amplifier, which William H Doherty of Bell Laboratories invented in 1936 (**Figure 6** and **Reference 1**). This amplifier has two RF paths. The RF does not just shuttle between a low-power stage and a high-power stage. The output-voltage swing in an RF amplifier should be close to the power-supply-rail voltage. The Doherty amplifier uses the second amplifier to change the apparent output impedance on the main amplifier. An amplifier feeding a transmission line faces an infinite output impedance if the second amplifier produces an identical signal on the other end of the line (**Figure 7**). Because both ends of the transmission line are equipotential, no current flows, and the line delivers no power. If you don't drive the secondary amplifier at all, then the output impedance that the first amplifier "sees" is the characteristic impedance of the transmission line. By extension of this principle, if you drive the secondary amplifier 180° out of phase from the first, then you are differentially driving the right side of the transmission line, and the apparent output impedance that the first amplifier sees is half the characteristic line impedance, increasing the delivered power. The main amplifier always swings near the output rails. If the design requires low-power transmission, the secondary amplifier increases the ap-

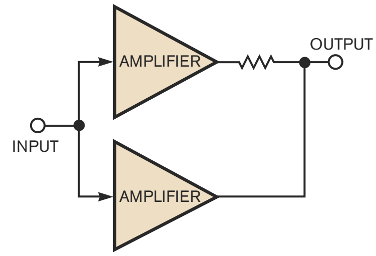

Figure 7 In this circuit, the same signal passes to both sides of a resistor, and the upper amplifier sees an infinite load. The amplifiers drive both sides of the resistor at the same amplitude, so neither amplifier sources any current or delivers power to the resistor. If the signal to each amplifier is 180° out of phase, the load that each amplifier perceives would be twice the resistor value. A Doherty amplifier uses this principle to vary output power and maintain efficiency.

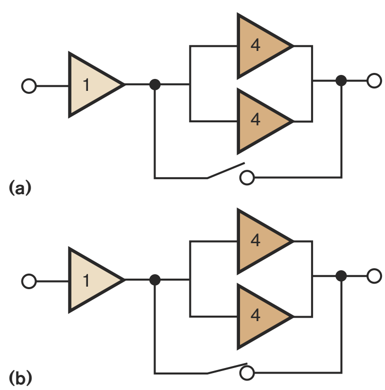

Figure 8 The low cost of handsets encourages the use of straightforward methods to improve efficiency. Avago makes amplifier modules that switch between high-power mode with output power greater than 16 dBM (a) and low-power mode with output power less than 16 dBm (b). The improvement in efficiency can add an hour of talk time.

parent output impedance that the main amplifier sees, and, for a given voltage swing near the rail, the amplifier delivers less current and, hence, less power.

The sophistication of the Doherty amplifier makes it a good fit for use in the base-station side of the cell-phone world. On the handset side, space and cost constraints are far more severe. In this case, you can use RF switches to switch gain blocks as necessary, providing substantial power savings. For example, Avago's CoolPAM (power-amplifier-module) RF devices provide cell-phone designers a way to maintain efficiency over wide output-power levels (**Figure 8**). You can use this straightforward technique instead of feeding the output stage with a dc/dc converter. Using the converters allows the RF-output stage to always operate near saturation and, hence, improve efficiency. However, dc/dc converters consume more space and have efficiency limitations of their own. Using the CoolPAM technology, Avago claims, can increase talk time to more than an hour, a compelling opportunity for cell-phone designers.

THE TROUBLE WITH MODELING

The quest for linearity with efficiency in RF-power amplifiers also affects the EDA tools for developing RF systems. Because these RF systems are inherently nonlinear, they share all the mathematical problems of other nonlinear systems. Using Spice and other circuit-simulation techniques may not apply and may be time-consuming because RF designs often require steady-state operation, a condition that may take billions of signal excursions to achieve. RF designers have typically resorted to black-box-modeling techniques, such as the use of S (scattering) parameters, to design systems. S parameters do not account for nonlinearity and do not model the bias points of the amplifier, however. To solve this problem, Agilent, which popularized S-parameter design, recently introduced X parameters, or polyharmonic-distortion modeling (**Reference 2**). These parameters combine the response of a linear system with the response due to the nonlinear factors. Agilent has provided several papers detailing this technique, and the inclusion of X-parameter simulation in Agilent's RF-design tools and the development of Agilent's test equipment that can characterize X parameters are sure to follow.

The design of RF-power amplifiers is becoming increasingly difficult due to the design requirements for new cell-phone-modulation schemes. The RF domain has long been the realm of intuitive design and experienced engineers. The demands on linearity and efficiency in these new designs only further accentuate the need for expertise when creating designs that work properly. The design effort is also spreading across disciplines. RF-, analog-, and digital-system designers all contribute to the performance of the signal chain. With experienced designers now getting access to sophisticated tools and instruments from EDA and test-equipment manufacturers, you can all look forward to even more amazing performance gains, all at significantly lower costs. EDN

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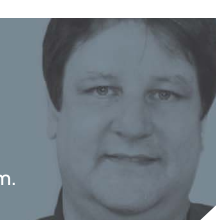

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BY RICK NELSON, EDITOR-IN-CHIEF • RON WILSON, EXECUTIVE EDITOR

CHIP SETS ARE EMERGING THAT ADD WIMAX CAPABILITY TO MOBILE PC AND CELL-PHONE APPLICATIONS, WHILE LAB AND PRODUCTION-TEST EQUIPMENT EVOLVES TO KEEP PACE.

LAYING SEAMLESS WIMAX FABRIC

WiMax (worldwide interoperability for microwave access) stands poised to extend coverage in PC networking and mobile-phone communications as semiconductor makers roll out WiMax chip sets and as test-equipment vendors offer the lab instrumentation and production ATE (automatic-test-equipment) systems necessary to test the chip sets and the products they populate. WiMax shows promise as a technology for PC networking as well as a potential cellular technology (see **sidebar** "WiMax markets and opportunities"). Paul Argent of Aeroflex expects WiMax to initially bring broadband-wireless access to laptops despite suggestions from WiMax Forum members that WiMax is a technology for multiple applications, including cellular telephony. Over the next two years, Argent says, WiMax will primarily provide high-speed data access to PCs in coffee shops as well as in moving vehicles.

Jennifer Stark, Agilent's WiMax business-team leader, cautions that you should not consider WiMax as a replacement for other broadband-wireless-access technologies. She segments wireless technologies by range—with personal-area networks, such as UWB (ultrawideband) and Bluetooth, operating at 10m or less; WLANs (wireless local-area networks) operating at 100m or less; and WiMax operating at three to 10 miles or more. As for WiMax's competing with WLANs, she expects them rather to complement each other, with appliances making the most effective connection based on conditions of the moment. For instance, WiMax will be the choice if you're on a train going 50 mph, she says; if you later find yourself in a stationary situation, WLAN might be the best choice.

WIMAX-CHIP TEST

To test WiMax chips in production volumes, ATE makers are adapting their RF-capable systems to handle WiMax-test requirements, and makers of bench- and rack-mount test equipment are tailoring their instrumentation to handle a potential onslaught of components, modules, and WiMax-compatible appliances. These vendors are also addressing the test needs of service providers that will install and maintain the WiMax infrastructure. Adam Smith, a business-development engineer at Verigy, says that WiMax test represents an evolutionary step from WLAN test, with WiMax imposing stricter requirements as designers try to cram ever more features into a tighter space. "From a test-equipment point of view," he says, "your equipment needs to have very good noise performance; it needs to be very sensitive." Agilent's Stark adds that WiMax's underlying OFDM (orthogonal-frequency-division-

multiplexing) scheme results in high peak-to-average power levels, putting a premium on highly accurate power-amplifier measurements.

Testing of WiMax silicon presents an instructive bundle of issues to chip designers and test engineers. On one hand, if WiMax is to reach wide acceptance, test costs—including the cost of silicon overhead to support testing—must be as small as possible. Ultimately, says Smith, someone will want to fit WiMax capability within a $99 mobile device. On the other hand, a number of factors militate against a fast, comprehensive test procedure. The WiMax standard is still not mature. Adjustments are by now small, but they still happen. More important, the standards reach only far enough to attempt to ensure interoperability at the system level. They make no demands on the implementation approach or on the signals passing between functional blocks in the implementation. Even more troubling, you may find that you don't have access to signals between functional blocks. Ken Harvey, senior product technologist at Teradyne, points out that, as WiMax chips become increasingly integrated, you'll find you might not have direct access to I (in-phase) and Q (quadrature) signals. "You'll go straight from RF to bits," he says.

Lacking standards against which to test the signal between the RF mixer and the ADC, and—potentially—access to that signal, you'll have to rely on system-level requirements, such as the EVM (error-vector magnitude) of the resolved signal and bit-error rate of the data stream. Agilent's Stark elaborates on this point. She divides the WiMax market into four segments: chips and components; modules, for which chip makers' reference designs sometimes substitute; appliances; and service providers. She concurs that EVM is a system-level spec that requires measurement at the appliance level but cautions that designers must be aware of component and module EVM of a power amplifier, for example, so that they can stay within an overall EVM budget. Ultimately, she says, test will play a key role as vendors try to differentiate their components in features, RF performance, and power consumption as they strive to fit WiMax capability within the tight constraints of appliances. Stark points out that WiMax-appliance vendors fortunately won't create brand-new devices that you've never seen before. The use case for WiMax, she says, is to add WiMax to currently available devices, such as laptops, PDAs (personal digital assistants), and cell phones.

AT A GLANCE

- WLANs (wireless local-area networks) and WiMax (worldwide interoperability for microwave access) should complement, rather than compete with, each other.
- ATE (automatic-test-equipment) makers are adapting their RF-capable systems to handle WiMax-test requirements, and makers of bench- and rack-mount test equipment are tailoring their instruments for an onslaught of components, modules, and WiMax-compatible appliances.
- WiMax standards reach only far enough to attempt to ensure interoperability at the system level.
- Designers must be aware of component and module EVM (error-vector magnitude) so that they can stay within an overall EVM budget.
- High-performance ATE lets you characterize silicon on the ATE itself, smoothing the transition to high-volume production test.

The Agilent E6651A WiMax test set supports protocol-conformance test as well as base-station emulation and RF-parametric measurements.

But just how a system, no matter how familiar, reaches adequate system-level performance standards varies depending on the baseband software, system design, and intended operating environment of that system. So, there is no straightforward translation between WiMax's system-performance specifications and testable behaviors on WiMax silicon.

The testing problem is easier in some functional blocks than others, however. The digital baseband, for instance, from a testing point of view, is just another fast signal processor. According to an Intel engineering spokesman, "WiMax silicon is not very different from any other SOC [system-on-chip] testing we perform at Intel. The part goes through Intel's strict product-reliability and qualification guidelines that include wafer testing, ESD [electrostatic-discharge] stressing, burn-in, and analog/mixed-signal testing across a broad range of temperature, environmental, and power-supply variability conditions. WiMax silicon can use the same DFT (design-for-test) techniques and hardware structures that are common in SOC design, such as at-speed scan, ATPG [automatic test-pattern generation], and logic and memory BIST [built-in self-test]. The process also includes package qualification, and silicon performance testing on multiple skew lots, as well as normal silicon lots."

Baseband silicon is a specialized, but still programmable, signal processor. It is either working correctly, or it isn't. Designers must adjust the software to the application, and that challenge is not a testing problem.

ANALOG SPACE

If you talk to a vendor of RF silicon, you get a different view. In the digital world, chip variations don't alter the performance of a device until they become so severe as to break the circuit. In the RF and analog domains, variations in the chip are variations in the chip's performance. As one old chestnut has it, you test digital circuits, but you characterize analog ones. This distinction changes the approach test engineers must take to an emerging technology such as WiMax.

"WiMax is all over the place right now," says Tom Gratzek, business director for the WiMax silicon program at Analog Devices. "There are different frequency bands, different bandwidth requirements, different baseband filtering schemes; everyone has an approach." The company offers WiMax front-end silicon, which includes the RF stages, mixers, ADCs, DACs, and some digital filtering. Gratzek says that Analog Devices tests the digital portions of the chips in the same way as it does any other digital circuitry: with scan-based BIST. After that, things get more complex, however.

"We have to examine the analog signal chain for defects," Gratzek says. "That by itself requires hundreds of milliseconds of test time. After that, the only approach we have found to predict how the chip will work in the customer's system is to stimulate the silicon at speed." This testing is not, Gratzek explains, a full characterization. Rather, the test program is an artful compromise that the company bases on the full characterization of skew lots in the engineering lab, on the ability of test engineers to elegantly check many degrees of freedom with a few tests, and on continuous feedback from the company's applications engineers who work on customers' designs. Analog Devices drives the receiver with 2-, 3-, and 4.9- to 5.9-GHz-band test signals and drives the transmitter with corresponding digital vectors. "We sweep three frequencies in each band," Gratzek says. "Unfortunately, that [approach] forces us onto mainframe RF testers, and it adds seconds of test time."

This approach is not unique. Infineon engineers report that they also generally stimulate their WiMax silicon at speed. They use a standard 64-QAM (64-state-quadrature-amplitude modulation) Rate 2/3 of a 3.5-MHz-bandwidth signal at 4 MHz as a starting point. But Infineon is seeing increasing pressure for customers with video-over-broadband applications to expand the bandwidth to 10 or even 20 MHz, causing changes from the silicon on up through the testing program.

Even moving to mainframe RF ATE isn't the whole solution, though. Gratzek says that Analog Devices has augmented its testers' already-formidable hardware with some custom spectral-analysis gear. That equipment also integrates some proprietary design features in the silicon and the device-under-test card to increase coverage and reduce test time. This allows the test team to sweep frequencies for an end-to-end test on the receiver side, for instance, driving the antenna inputs to the LNA (low-noise amplifier) and analyzing the output stream from the ADC for EVM and noise figures.

These top-line numbers give the company a go/no-go indication and more on each die. For instance, the engineers can infer the SNR (signal-to-noise ratio) and linearity of the ADC from the end-to-end test. But the test team can extract even more detailed information as well, due to the high degree of digital configurability of the RF design. "We can manually control the automatic-gain-control loop, and we do so during test," Gratzek says. "We can also disembed the digital filters on the output of the chain to examine the raw digital data. And we can force the analog filters to specific characteristics, step through the gain settings on the LNA, and so forth." This approach allows the test team to move, if necessary, from the end-to-end test to an almost diagnostic level of examination while still on the production-test head.

This flexibility comes in handy. "We are delivering WiMax chips to all sorts of customers' evaluation boards, and

WIMAX MARKETS AND OPPORTUNITIES

Embedded mobile WiMax in mobile PCs will drive the emerging WiMax chip set market through 2012, says In-Stat (Reference A). "The market-research company predicts that Intel's combination Mobile WiMax (interoperability for microwave access) and Wi-Fi Echo Peak module, which will launch as an option to the company's Montevina mobile processor platform in 2008, will drive the adoption of embedded WiMax into mobile PCs. WiMax CPE (customer-premises equipment), external clients, and dual-mode cellular/WiMax handsets will also help drive WiMax-chip-set volumes through 2012, the company reports.

"The total WiMax user terminal-chip-set market will reach almost $500 million in 2012, growing from $27 million in 2007," says Gemma Tedesco, In-Stat analyst, in a press release. "Furthermore, WiMax base-station-semiconductor revenues are expected to be approximately $1.4 billion in 2012, compared to $130 million in 2007."

In a separate report, In-Stat says that, from a mobile operator's perspective, mobile WiMax provides more of a service complement than a competitive threat (Reference B). The company notes that the mobile standard for WiMax has been the subject of debate since its inception, with debaters falling into two camps.

"One camp led by select equipment vendors with no stake in WiMax has taken an either/or approach to discussing mobile WiMax," says Daryl Schoolar, In-Stat analyst, in a press release. "Any gain by WiMax comes at the expense of other 3G data technologies. In the other camp, infrastructure vendors, such as Alcatel-Lucent, Motorola, and Nokia Siemens, see a world where multiple mobile wireless-broadband technologies will coexist. In-Stat believes that this camp's view will prevail."

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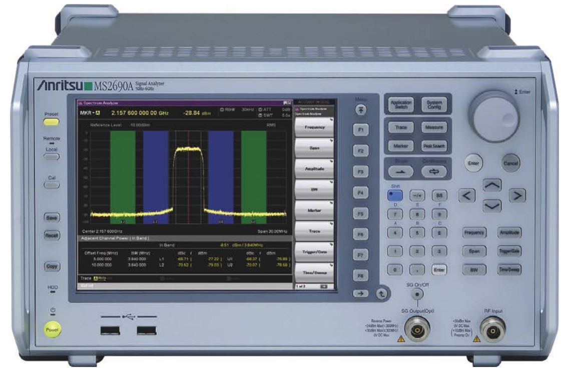
The CMU270 single-instrument production tester from Rohde & Schwarz makes signaling and nonsignaling measurements of WiMax mobile stations and customer-premises equipment.



Anritsu M2690A/M2691A signal analyzers operate from 50 Hz to 6 GHz and can measure the transmitting power of mobile-WiMax devices.

they use the silicon in many ways," Gratzek says. "Our applications engineers feed use data back to the test team, and we try to adjust the tests to anticipate the sensitivities of a … customer application. For instance, many customers change the filter settings to get the EVM they want on a … board and antenna configuration. We try to adapt to that [configuration]." This approach means that the application-support team reserves time on the test floor for development purposes.

Commercial-test companies are working to streamline WiMax test. ATE vendors including Advantest, Teradyne, and Verigy are tailoring their systems to test WiMax devices in multisite configurations. Verigy's Smith says nothing is magical about WiMax. UWB is dealing with new spectra, but WiMax aims to make more efficient use of the allocated spectrum, he says. WiMax test is well within the capabilities of his company's Port Scale RF instrument, which Verigy introduced last summer for the V93000 system. Similarly, Advantest's 12GWS-GA RF module, which the company introduced last fall for its T2000 test system, and Teradyne's UltraWave, which the company introduced in March, will handle WiMax-chip test.

Semiconductor-ATE systems have typically focused on high throughput without necessarily providing the performance of bench-top and rack-mount instrumentation, but the advent of WiMax is changing that scenario, says Teradyne's Harvey. Measurement requirements are becoming so stringent, he says, that ATE instruments must approach bench and rack versions in measurement capability. He cites an additional advantage of high-performance ATE: It lets you characterize silicon on the ATE itself, smoothing the transition to high-volume production test.

Companies that provide test equipment for WiMax modules and appliances as well as components include Anritsu, Agilent Technologies, Aeroflex, Tektronix, and Rohde & Schwarz, all of which make general-purpose test and measurement equipment that can perform tests on WiMax systems as well as dedicated WiMax boxes and software.

Tektronix, for example, offers the K1297-G35 WiMax protocol analyzer, which provides protocol simulation, emulation, and monitoring. In addition, Tektronix offers for its real-time spectrum analyzers the RSA-IQWiMax software, which can help detect, diagnose, and resolve WiMax-design errors. Rohde & Schwarz offers the CMU270 single-instrument production tester as well as the TS8970 WiMax-radio-conformance-test system. Anritsu offers bench-top signal-generation and analysis instruments, such as the MS2690A signal analyzer and MG3700A vector-signal generator, as well as the handheld MS2724B spectrum analyzer, which can make fixed- and mobile-WiMax measurements in the field.

Aeroflex offers WiMax-test equipment in PXI (PCI-extensions-for-instrumentation) and traditional rack-and-stack formats for testing WiMax base stations and mobile devices "from birth to death," says Argent of Aeroflex. He notes that, before vendors submit their WiMax devices to WiMax Forum-certification labs, they would benefit from doing their own precertification tests to help ensure that their devices pass the first time. When WiMax Forum labs are charging approximately $500 per hour, he says, customers will want to have maximum confidence that their products will pass quickly.

Agilent's offerings extend from the EEsof division's ADS (Advanced Design System) design and simulation software to WiMax-drive-test systems. Along the way, the company offers a complement of signal-generation and -analysis equipment, which can link to ADS through Agilent's Connected Solutions technology, as well as WiMax protocol analyzers and logic analyzers for baseband development and troubleshooting.

Test cost will be paramount—for chips, modules, appliances, and infrastructure installation and maintenance. Gratzek of Analog Devices summarizes the cost issue from a chip maker's perspective: "On our GSM [global-system-for-mobile-communication]-product line, we were able to substantially reduce the test cost as the market matured," he says. "We aren't at that stage yet with WiMax, but we have planned for it. We designed our ATE strategy from the beginning with an end cost point in mind and a path to get there. We may well reduce the test cost by a factor of three as the technology matures." EDN

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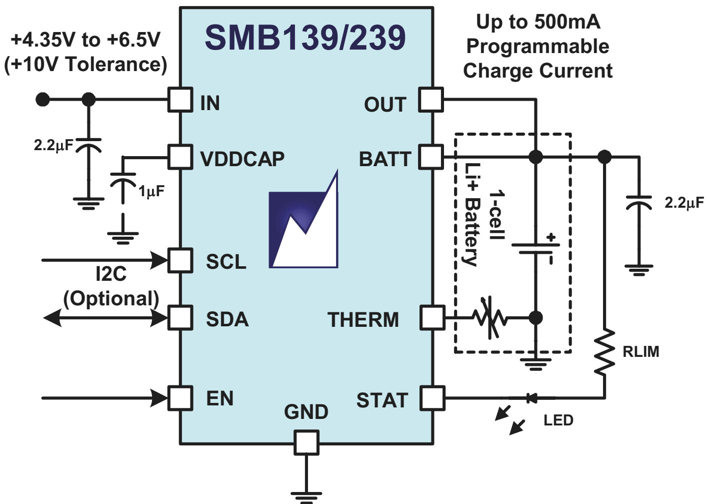

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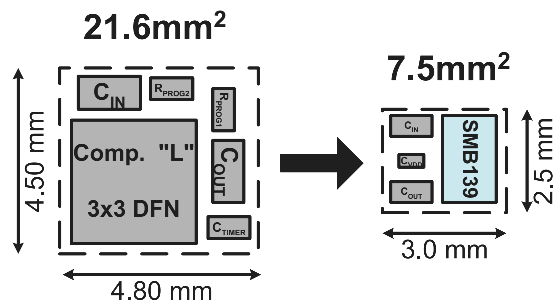

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CurrentPath™ Control	X			
USB On-The-Go Power	X	X		
Low-Battery Recovery Mode	X			
I2C Interface	X	X	X	X
Programmable Float Voltage	X	X	X	X
Programmable Charge/Term. Current	X	X	X	X
Programmable Input Current Limit	X	X		
Input/Battery OV/UV	X	X	X	X
Hardware Safety Timer	X	X	X	X
Software Watchdog Timer	X	X		
Battery Thermal Protection	X		X	X
IC Thermal Protection	X	X	X	X
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In a conventional diode-rectified flyback converter, the output diode rectifier is a substantial power-loss contributor. The average current in the output diode is equal to the dc output current, and the peak current can be several times higher, depending on the duty cycle. The forward-voltage drop of the diode is typically 0.5V for Schottky diodes and 0.8V for standard PN-junction diodes. This large forward-voltage drop leads to relatively high losses in the diode and a substantial reduction in efficiency. Replacing the diode with a synchronous MOSFET significantly reduces these conduction losses. **Figure 1** illustrates how you can convert a standard diode-rectified flyback supply into a self-driven-synchronous-flyback supply.

In the self-driven-synchronous flyback, an N-channel MOSFET replaces the output diode, and you must add a winding to the power transformer to generate the synchronous-gate-drive signal. The low on-resistance of the synchronous MOSFET yields much less conduction loss than the output-diode rectifier, significantly improving the efficiency at high load currents.

There is a fundamental difference between the operation of a diode-rectified flyback and a synchronous flyback. **Figure 2** shows the key waveforms. The output diode in the diode-rectified flyback prevents the transformer secondary current from flowing backward. At light loads, this condition results in DCM (discontinuous-current-mode) operation in which the transformer's secondary current completely discharges into the output at the end of each cycle. The synchronous MOSFET allows current to continue to flow in the negative direction and forces the synchronous flyback to always operate in CCM (continuous-current mode) regardless of load current. This situation is generally beneficial in that the control loop gain does not decrease as it does when it transitions into DCM operation, thereby maintaining full dynamic performance, even at zero load. The use of synchronous MOSFETs has a negative impact on zero- or light-load efficiency, because relatively large ac cur-

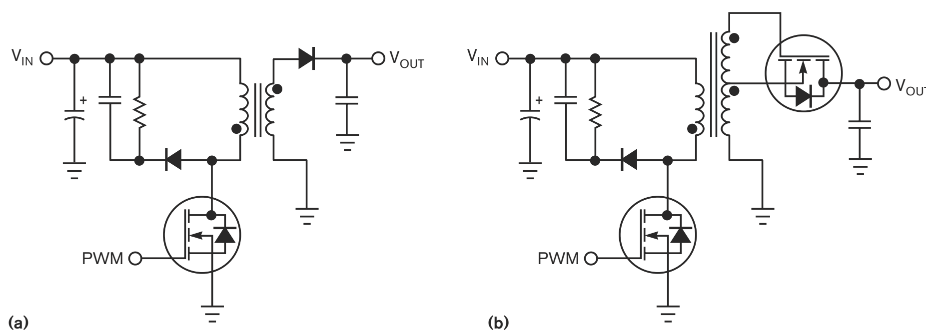

Figure 1 Replacing the output diode with an N-channel MOSFET and adding a winding to the power transformer to generate the synchronous-gate-drive signal can convert a standard diode-rectified flyback supply (a) into a self-driven synchronous-flyback supply (b).

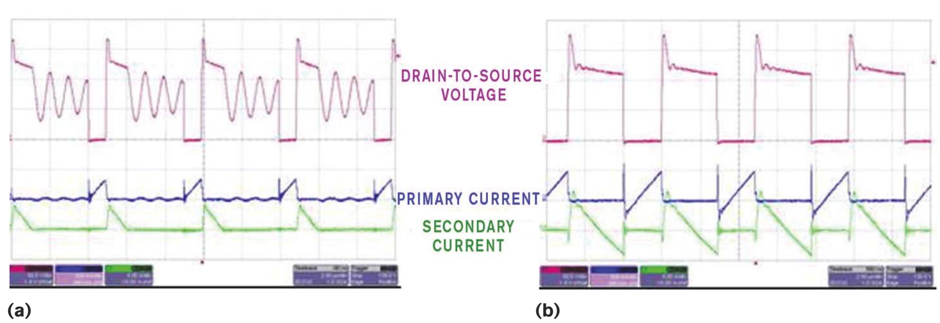

Figure 2 The output diode in the diode-rectified flyback prevents the transformer secondary current from flowing backward. At light loads, this situation results in discontinuous-current-mode operation in which the transformer's secondary current discharges completely into the output at the end of each cycle (a). The synchronous MOSFET allows current to continue to flow in the negative direction and forces the synchronous flyback to always operate in continuous-current mode, regardless of load current (b).

rents flow with little or no net dc-output current. Transformer and primary-MOSFET switching losses associated with these circulating currents are larger than those in the diode-rectified flyback, whose currents decrease in amplitude at light loads.

Although the synchronous MOSFET significantly lowers conduction losses, it introduces gate drive, switching, and shoot-through losses that are not present in the diode-rectified flyback. Gate-drive losses result from the capacitance of the MOSFET gate that charges and discharges during each switching cycle. At the turn-on and turn-off transitions of the MOSFET, switching losses occur as the drain-to-source voltage and the drain current exhibit overlap. Shoot-through occurs because the primary switch must turn on before the secondary FET can start to turn off. This situation places a short circuit across the transformer during switching and can lead to substantial power loss. In the self-driven synchronous flyback, the primary-MOSFET turn-on commands the synchronous-MOSFET turn-off. Hence, it is impossible to eliminate the shoot-through currents when the power transformer directly drives the synchronous MOSFET. A self-driven synchronous MOSFET must have fast-turn-off delay and fall times to minimize shoot-through losses. Although a properly designed synchronous MOSFET introduces additional switching losses, the conduction losses are typically substantially lower than the diode-rectifier-forward-drop losses. This one benefit alone typically outweighs all synchronous MOSFETs' negatives.

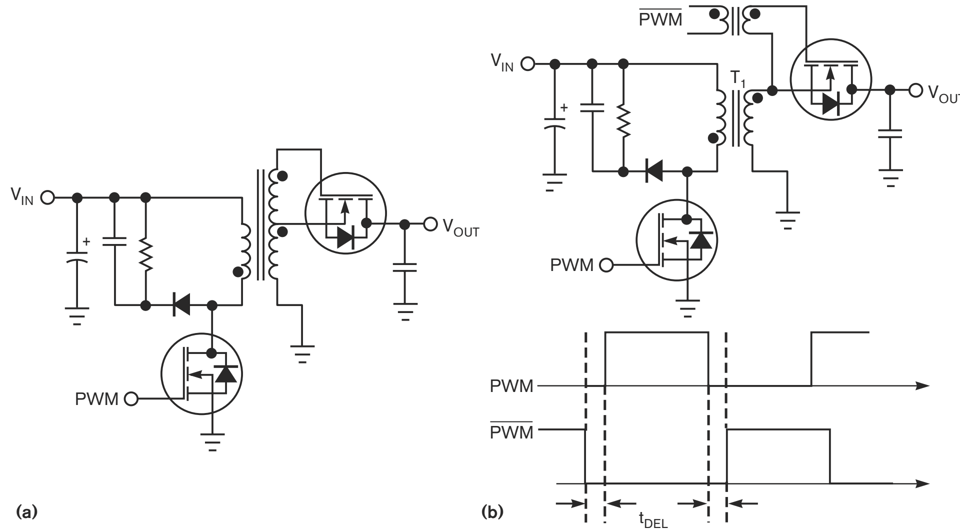

Figure 3 Adding an isolated gate-drive signal with programmable delays to the synchronous flyback (a) can eliminate shoot-through losses (b).

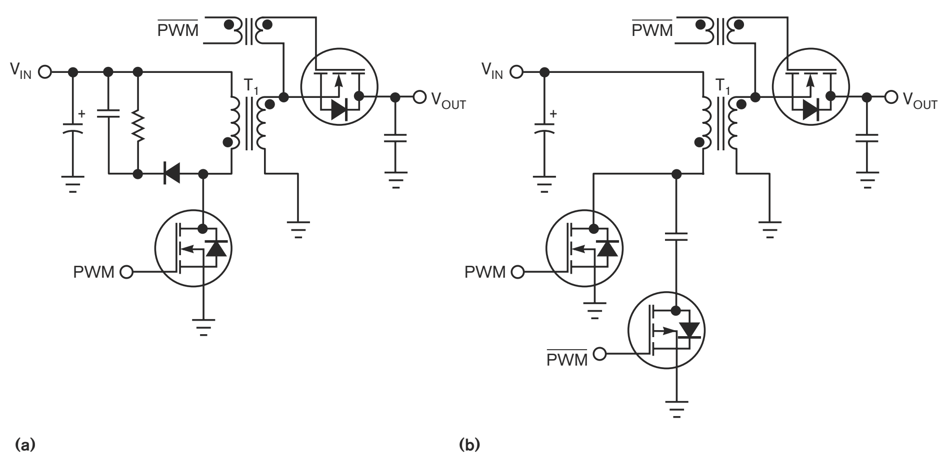

Figure 4 In the active-clamp flyback (a), the clamp capacitor captures the leakage energy, and the system recirculates it to the load and back to the input, resulting in a virtually lossless snubber (b).

Figure 3 shows how you can add an isolated gate-drive signal with programmable delays to the synchronous flyback to eliminate shoot-through losses. The device achieves isolation and level-shifting through a gate-drive transformer. A PWM controller with complementary drive outputs and adjustable delays, such as the UCC2897, is necessary to control the primary- and secondary-side synchronous MOSFETs. The delays must be long enough to ensure that the synchronous MOSFET is fully off before the primary MOSFET switches on. Excessive delay causes body-diode conduction on one or both of the MOSFETs and leads to excess power loss. Because the optimal dead time depends on the primary- and secondary-MOSFET delay, transition speed, power-transformer-leakage inductance, and gate-drive circuit, a controller with adjustable delay is critical to minimizing losses.

Figure 4 illustrates how to further improve the efficiency and take advantage of the synchronous-MOSFET-gate-drive signal to control an active primary snubber. This configuration

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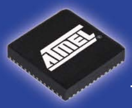

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is often called an active-clamp flyback. In the previous **figures**, the design employed a snubber to reduce the voltage spike on the drain-to-source voltage of the primary MOSFET. The spike occurs at turn-off of the primary MOSFET and is due to the leakage energy in the primary winding of the transformer. The RCD (resistor-capacitor-diode) snubber dissipates this energy in its snubber resistor. In the active-clamp flyback, the clamp capacitor captures the leakage energy, and the system recirculates it to the load and back to the input, resulting in a virtually lossless snubber. **Figure 5** shows the drain-to-source voltage waveforms of an RCD snubber versus an active clamp. The active clamp eliminates the high-frequency spike. In addition to virtually eliminating the leakage losses, the design significantly reduces switching losses and EMI (electromagnetic interference). In many cases, the active-clamp snubber allows the use of a lower drain-to-source-voltage-rated primary MOSFET, which can further reduce losses and possibly reduce the cost of the MOSFET.

Figure 6 shows how much each upgrade to the diode-rectified flyback improves the efficiency of a real-world design. The power supply converts a telecom 48V-dc input to a 3.3V output with a maximum load current of 3.5A. Converting from a diode rectifier to a self-driven-synchronous-flyback device improves the maximum load efficiency by more than 7% but decreases the light-load efficiency below an output current of 1A. This situation occurs because of the gate-drive, switching, and shoot-through losses that the synchronous MOSFET

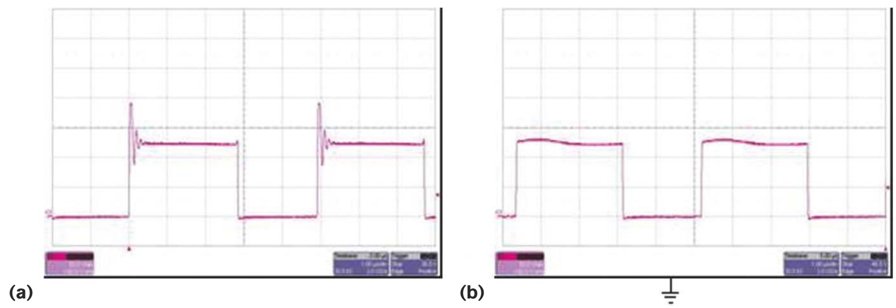

Figure 5 The drain-to-source-voltage waveforms of a programmable dead-time synchronous flyback circuit employ an RCD snubber (a) and an active clamp (b). The active clamp eliminates the high-frequency spike. In addition to virtually eliminating the leakage losses, this approach significantly reduces switching losses and EMI.

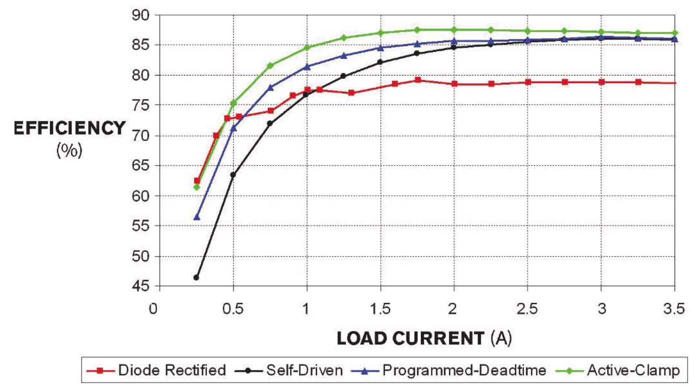

Figure 6 Using a power supply that converts a telecom 48V-dc input to a 3.3V output with a maximum load current of 3.5A as an example, each upgrade to the diode-rectified flyback improves the efficiency on a real-world design.

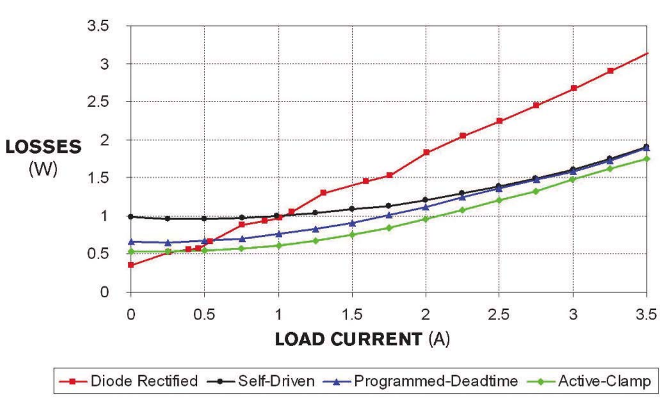

Figure 7 Introducing a programmable dead-time delay increases the light-load efficiency significantly by eliminating the shoot-through losses. The full-load efficiency remains nearly identical, because other circuit losses dominate the synchronous MOSFET losses. Implementing the active clamp increases the efficiency of the 3.3V supply across all loading conditions.

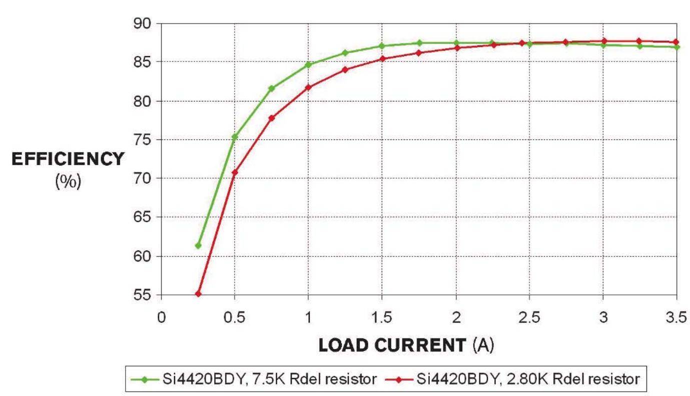

Figure 8 The delay resistor determines the dead time. In some situations, you may have to choose between maximizing efficiency at light loads or maximum load by selecting the appropriate delay-resistance value.

introduces. These losses become a larger percentage of the total losses at light loads and consequently decrease light-load efficiency (**Figure 7**). Introducing a programmable dead-time delay significantly boosts the light-load efficiency by eliminating the shoot-through losses. The full load efficiency remains nearly identical, because other circuit losses dominate the synchronous-MOSFET losses. Finally, implementing the active clamp increases the efficiency of the 3.3V supply across all loading conditions.

Figure 8 shows two delay settings in the active-clamp circuit and how they affect the efficiency at different loading conditions. A longer delay, which you program on the UCC2897 by using a larger value for a delay resistor significantly improves the light-load efficiency by decreasing the shoot-through losses at light load. But this longer delay also increases the synchronous MOSFET's body-diode conduction time and, at full load, reduces the efficiency by about 1%. The full-load synchronous-MOSFET body-diode-conduction losses dominate the shoot-through losses when using a lower delay resistance. In some situations, you may have to choose between maximizing efficiency at light loads or maximum load by selecting the appropriate delay-resistance value. **Figure 9** shows the active-clamp-flyback-power supply implementing all of the efficiency-improving techniques. This configuration yields nearly a 10% efficiency improvement at maximum load and has nearly the same light-load-efficiency performance as the original diode-rectified design. EDN

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AUTHORS' BIOGRAPHIES

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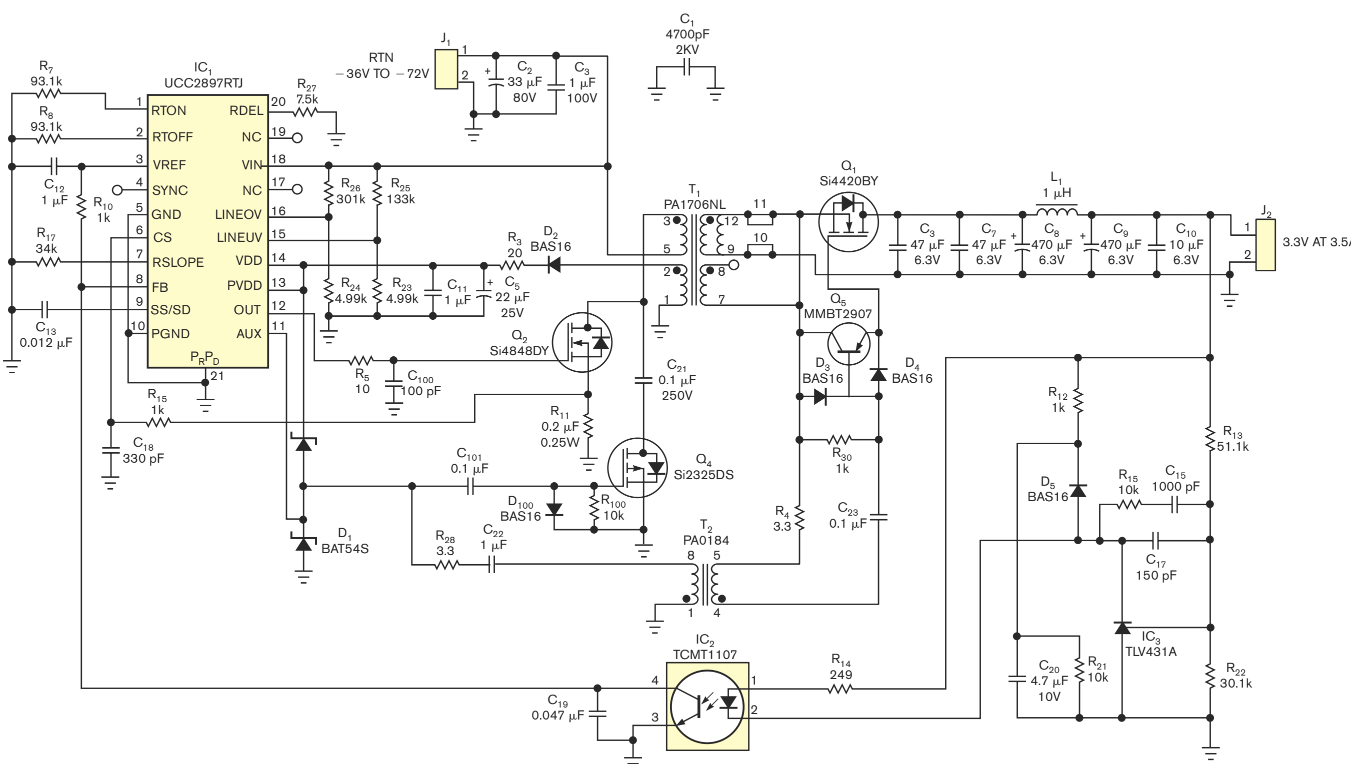

Figure 9 The active-clamp flyback power supply implements all of the efficiency-improving techniques, yields a nearly 10% efficiency improvement at maximum load, and has nearly the same light-load efficiency performance as the original diode-rectified design.

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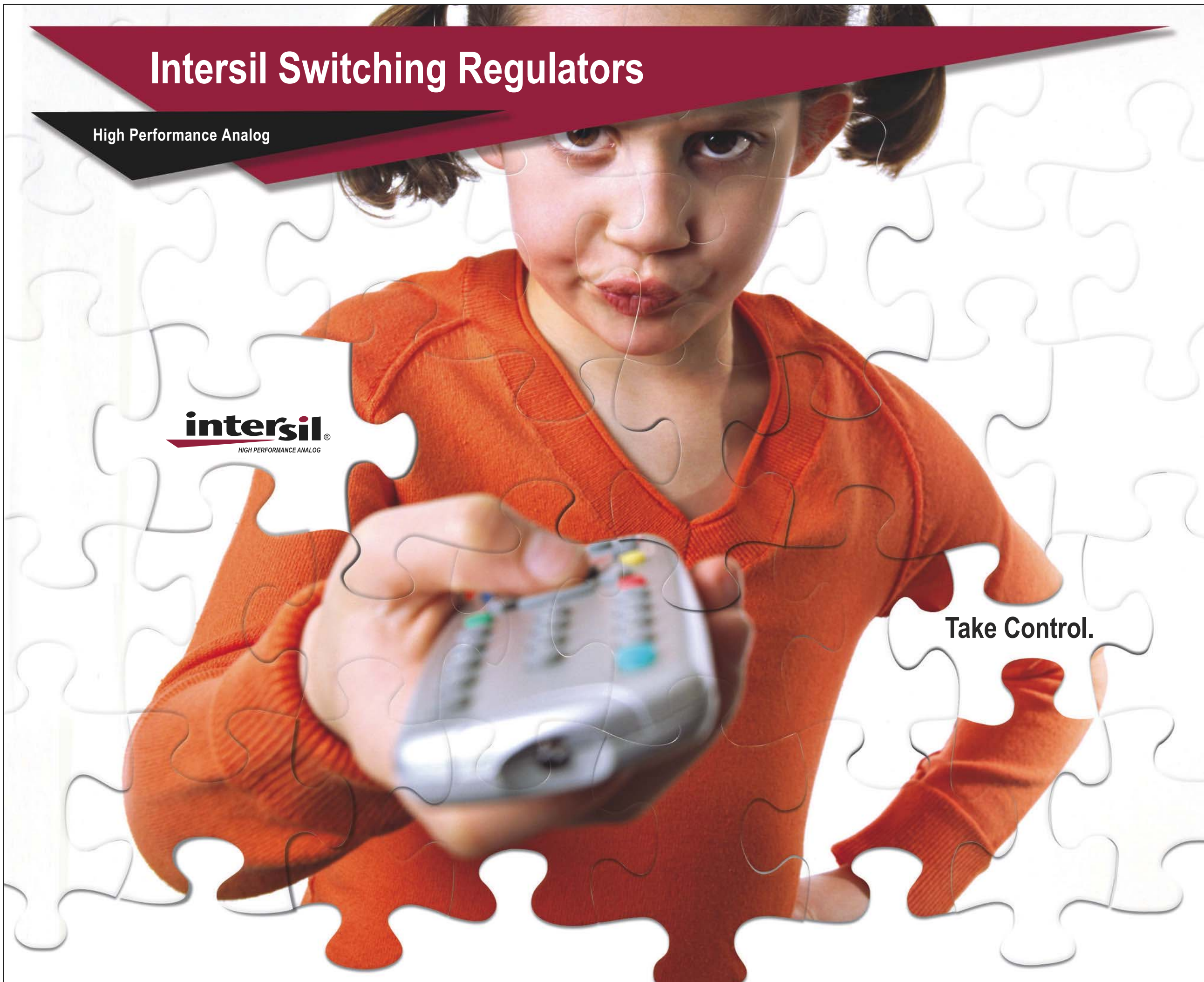

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1	0	4A	LX1, LX2, LX3, LX4	2A	LX5, LX6
0	1	5A	LX1, LX2, LX3, LX4, LX6	1A	LX5
0	0	2A	LX1, LX2, LX3, LX4, LX6	4A	LX3, LX4, LX5, LX6
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X	X	1A	LX2	5A	LX1, LX3, LX4, LX5, LX6

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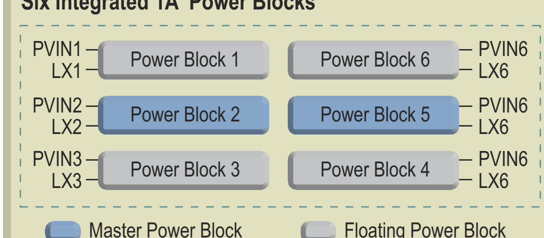

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BY SHAKER SARWARY AND SAURABH VERMA • ATRENTA INC

Critical clock-domain-crossing bugs

AWARENESS OF CDC ISSUES, ALONG WITH THE USE OF GOOD DESIGN PRACTICES AND PROVEN EDA TOOLS FOR CDC VERIFICATION, CAN AVOID COSTLY SILICON RE-SPINS AND SIGNIFICANTLY IMPROVE TIME TO MARKET.

Today's SOC (system-on-chip) designs have dozens of clocks, many of which are asynchronous. This design approach facilitates the convergence of digital-audio, video, wireless, and networking applications in a single chip. CDCs (clock-domain crossings) can cause difficult-to-detect functional failures in SOCs involving multiple asynchronous clocks. Simulation and static-timing analysis often do not detect issues such as metastability and the coherency of correlated signals' CDCs; as a result, these issues often end up as bugs in silicon. Unfortunately, most relevant literature does not adequately cover some of these critical CDC issues, and designers learn about them only after making costly mistakes. Two of the most common and critical issues involving CDCs are improper sequencing of data/enable in enable-based synchronization and data coherency due to the convergence of signals.

ENABLE-BASED SYNCHRONIZATION

A receiver flip-flop output can become metastable if it violates the data/reset setup-and-hold times. This scenario can arise when the transmitter—the source of data—and the receiver flip-flop are in asynchronous-clock domains. To avoid such issues, designers use synchronizers that isolate metastability and deliver a clean signal to the downstream logic. A synchronizer can be a simple double flip-flop. Designers commonly use this technique for a control signal's CDCs. In a data transfer across clock domains, the data is first set up; then, a control signal that synchronizes with the destination domain travels to the destination to enable data capture. Although this data-transfer technique across clock domains is a common and proven technique, it involves pitfalls that require special attention. This technique relies on data to be stable when you assert an enable (**Figure 1**).

Having too low a margin between the data you are setting up and the enable you are asserting may corrupt the data transfer. A good way to prevent such problems is to design a full handshake when you set up the data. In this approach, you assert and synchronize the request in the destination domain and adequately assert an acknowledge to let the next data load occur. This approach might add a few cycles of latency, but it avoids functional failures.

Glitches are other sources of worry across clock domains. Typically, any combinational logic may be subject to short-lived glitches. These issues are generally harmless because they resolve themselves when you activate the next clock edge. Although these issues are not problematic for synchronous transfers, a glitch may occur with asynchronous crossings if you activate a destination clock. The design may therefore receive a glitch as a pulse, causing a functional failure. For this reason, it is important to avoid using any combinational logic that may cause glitches on a CDC path. You

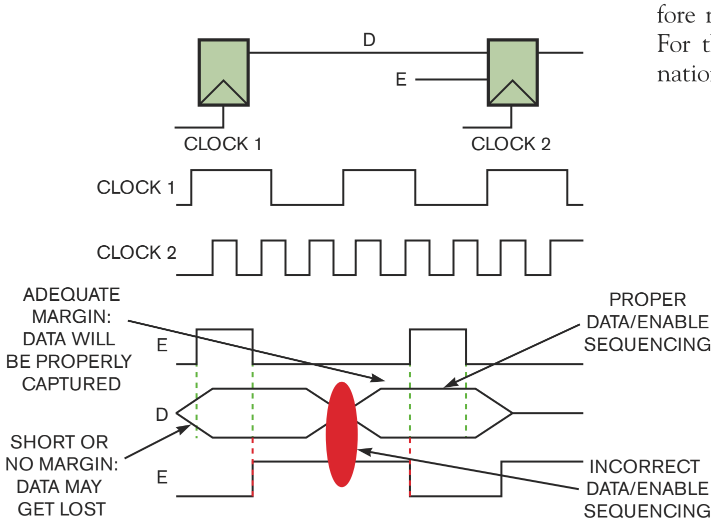


Figure 1 In a data transfer across clock domains, the data must be stable when enable is asserted. Too short of a margin between data setup and enable assertion can result in data corruption.

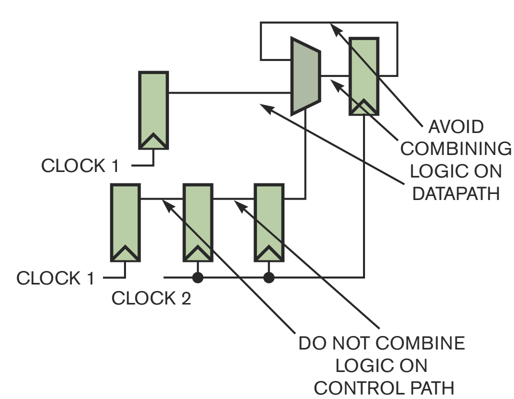
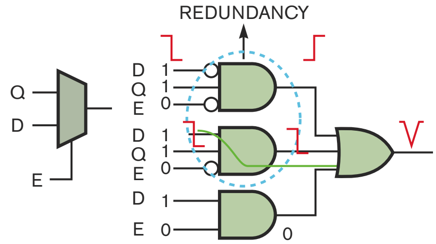


Figure 2 A good design practice is to avoid using any logic, except the recirculation-multiplexer logic, which is part of the enable flip-flop, on the datapath CDCs.



(a) (b)

Figure 3 You can map a simple, glitch-free multiplexer (a) with AND and OR gates that can create glitches (b).

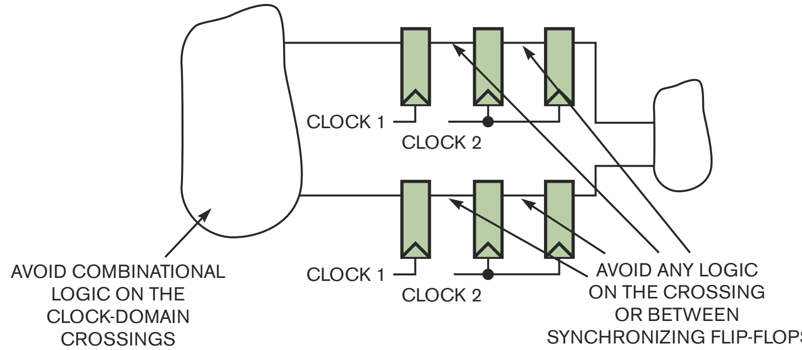


Figure 4 Any glitch in the Gray encoder may cause a functional failure in the design.

should perform any computation either before crossing clock domains or after the destination domain captures the signals.

Glitches may affect both control and data CDCs. In a data transfer, a glitch may affect the enable line or the data line; both present risks affecting safe data transfer. You must synchronize the enable logic in the destination domain and avoid using combinational logic after synchronization. Glitches on the datapath may be harmful, too. A good design practice is to avoid using any logic, except the recirculation-multiplexer logic, which is part of the enable flip-flop, on the datapath CDCs (**Figure 2**).

Although this data-synchronization scheme is the most common, many variations of enabled-data crossing involve an enable signal with combinational logic. Occasionally, designers use an enabled AND instead of a multiplexer or combine the multiplexer with other combinational logic on the datapath. They rely on the enable signal to ensure that data synchronously transfers to the destination and that glitches do not occur. As designers become more creative and use extra logic in enabled-data crossings, they expose their designs to glitch risks that are difficult to detect. To comprehend these risks, consider a simple example of a glitch-free multiplexer; you can implement this multiplexer so that it can create a glitch. Downstream tools, such as synthesis, optimization, and technology mapping, can transform the circuit and introduce logic that can cause a glitch and thus cause a functional failure. You can map a simple, glitch-free multiplexer with AND and OR gates that can create glitches (**Figure 3**).

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Although this transformation may seem unlikely with a stand-alone multiplexer, it may well occur if you introduce more logic on the datapath. Synthesis and optimization tools may identify opportunities to increase timing performance, reduce area, or decrease power consumption by combining multiplexer logic with other logic on the path; however, these tools may also create a final implementation prone to glitches. To avoid such problems, you should control the use of these tools to avoid such transformations. Unfortunately, designers often fail to consider these details when creating and implementing a design. Furthermore, a glitch is not an easily predictable event; simulation or static-timing verification cannot detect a glitch on an asynchronous crossing. Once the symptom appears in silicon, it is difficult to perform a root-cause analysis. It takes significant effort and time to link silicon failures to a glitch on a CDC. Static-CDC analysis is better for systematically catching and reporting such issues and avoiding costly silicon re-spins.

	BINARY COUNT	GRAY COUNT
0	000	000
1	001	001
2	010	011
3	011	010
4	100	110
5	101	111
6	110	101
7	111	100

BAD GRAY CODE IF COUNT GOES TO FIVE

GOOD GRAY CODE IF COUNT GOES TO SEVEN

Figure 5 A Gray encoder targeting counting from zero to seven for a full 3-bit counter will fail when the pointer moves from five to zero.

DATA COHERENCY

Another critical issue involving asynchronous clocks is the coherency problem due to convergence of independently synchronized signals. CDCs introduce latency and cycle-level uncertainty, even with synchronized crossings. Although synchronizers isolate metastability and ensure that a "clean" signal travels to downstream logic, they cannot prevent latency. Coherency problems occur when two correlated, separately synchronized signals cross clock domains; each synchronizer introduces a different latency factor due to the CDC. If one of the signals captures a transition, metastability settles to the correct value in the first cycle, whereas the other signal captures a transition in the next cycle. That is, metastability settles to an incorrect value, and you must wait for the next clock cycle to capture the transition. Then, you will observe an incorrect set of values at the destination for at least one cycle. If the signals represent a state variable, then you will observe an unknown or unwanted state at the destination. This unknown state causes a functional failure in the design.

This problem is one of the most common in CDC, and it is becoming more important as designs become larger. Design reuse and IP (intellectual-property) integration may create convergences of which designers may be unaware. To avoid coherency problems—assuming that you know the convergences—you should use correlated signals so that they change values at different times. You must use Gray encoding to correlate signals that are CDCs. This scenario occurs when FIFO point-

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LT3474/-1	Buck	400:1 PWM	4 to 36	9/25	1.00	TSSOP-16E
LT3475/-1	Dual Buck	3000:1 PWM	4 to 36 (40 Max.)	9/25	1.50 x 2	TSSOP-20E
LT3476	Quad Buck, Boost, Buck/Boost Mode	1000:1 PWM	2.8 to 16	36	1.00 x 4	5mm x 7mm QFN-38
LT3477	Buck, Boost, Buck/Boost Mode	DC/PWM	2.5 to 25	40	2.00	4mm x 4mm QFN-20, TSSOP-20E
LT3478/-1	Buck, Boost, Buck/Boost Mode	3000:1 PWM	2.8 to 36 (40 Max.)	40	4.00	TSSOP-16E
LT3486	Dual Boost	1000:1 PWM	2.7 to 24	35	0.10 x 2	3mm x 5mm DFN-16
LT3496	Triple Buck, Boost, Buck/Boost Mode	3000:1 PWM	3 to 30 (40 Max.)	45	0.50 x 3	4mm x 5mm QFN-28
LT3517/18	Buck, Boost, Buck/Boost Mode	5000:1 PWM	3 to 30 (40 Max.)	45	1.0/2.0	4mm x 4mm QFN-16
LT3590	Buck Mode	200:1 PWM	4.5 to 55	n/a	0.05	2mm x 2mm DFN-6, SC-70
LT3595	Buck Mode	3000:1 PWM	4.5 to 45	n/a	0.05 x 16	5mm x 9mm QFN-56
LT3755/56	Buck, Boost, Buck/Boost Mode	3000:1 PWM	4.5 to 40/6 to 100	60/100	Ext. FET	3mm x 3mm QFN-16, MSOP-16E
LTC®3783	Buck, Boost, Buck/Boost Mode	3000:1 PWM	3 to 36	40	Ext. FET	4mm x 5mm DFN-16, TSSOP-16E

*Actual output current will depend on V_{IN}, V_{OUT} and topology.

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ers cross clock domains to compute empty and full flags. You Gray-encode the binary counters, transfer to the other domain, and then convert the counters back to binary before using them. Occasionally, designers access pointers in a FIFO block to do empty/almost-empty or full/almost-full flag calculations. This practice may create CDCs, convergences, or both that a designer may overlook. Adopting standard practices prevents the introduction of CDC bugs into the design.

Gray-encoding circuitry seems simple; however, errors can easily slip into a design. You must Gray-encode and register the signals before crossing clock domains. Sending Gray-encoded signals directly to the destination domain defies the purpose. Furthermore, any glitch in the Gray encoder may cause a functional failure in the design (**Figure 4**).

Another subtle issue is mismatch between Gray-encoding assumptions and the binary-counter range. Designs sometimes fail when a designer expects a Gray counter targeting the full range of a 4-bit counter to count to lower counts and loop back to zero. For example, a designer can build the write pointer of a six-layer-deep FIFO to count from zero to five and loop back to address zero. A Gray encoder targeting counting from zero to seven for a full 3-bit counter will fail when the pointer moves from five to zero (**Figure 5**).

Designing a Gray encoder may give a false sense of security if you fail to account for these details. Both junior and experienced designers may face such issues. There are a large number of corner-case problems in CDC, and it is difficult for any designer to pay attention to all the details, especially when under tight schedule pressure. The best way to catch these issues is to approach them with a systematic methodology that has concise metrics. Static-CDC verification has recently emerged as an accepted approach to achieve this goal. This approach targets metastability, convergence, and other CDC issues that traditional verification tools, such as simulation and static-timing verification, do not cover. Static-CDC verification successfully targets corner cases that designers may overlook. Furthermore, it provides a systematic-verification approach that can fit into any design flow as part of the verification-sign-off tool suite. EDN

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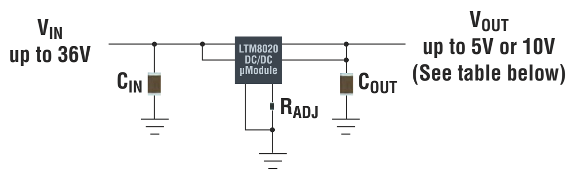

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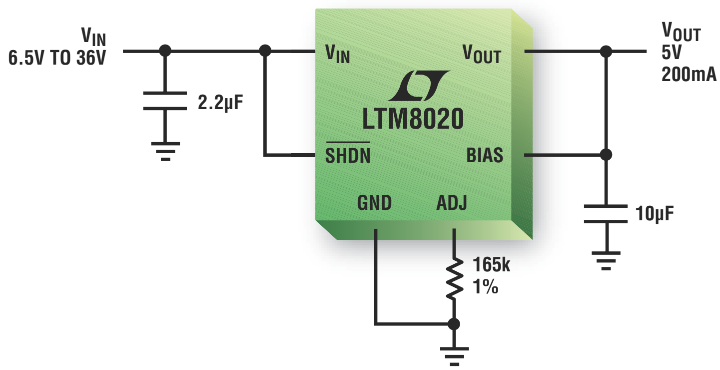

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I_{OUT}	200mA	500mA	1A	2A
Size (mm)	6.25 x 6.25 x 2.3	6.25 x 11.25 x 2.8	11.25 x 9 x 2.8 Pin Compatible	

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µModule Buck-Boost Regulators Offer a Simple and Efficient Solution for Wide Input and Output Voltage Range Applications

Design Note 438

Jian Yin and Eddie Beville

Introduction

An increasing number of applications require DC/DC converters that produce an output that falls somewhere within the input voltage range. The problem is that conventional buck-boost converter topologies, such as SEPIC or boost followed by buck, are complex, inefficient and consume a relatively large board area. Linear Technology offers 4-switch-topology buck-boost regulators that significantly improve efficiency and save space, but a complete regulator design still requires a number of external components and meticulous board layout decisions related to electrical and thermal considerations. The next clear step to simplify the design is a modular approach—a buck-boost regulator system in an IC form factor. The LTM4605 and LTM4607 µModule™ buck-boost regulators take that approach. Each requires only one external inductor and a single sensing resistor to produce a compact, high performance, high efficiency buck-boost regulator with exceptional thermal performance.

High Efficiency

The LTM4605 and LTM4607 are high efficiency switch mode buck-boost power supply modules. The LTM4605 can operate over an input voltage range of 4.5V to 20V and support any output voltage within the range of 0.8V to 16V, set by a single resistor. As shown in Figure 1, the LTM4607 supports 4.5V to 36V inputs and outputs of 0.8V to 16V. Both can provide 92% to 98% efficiency over the wide input range. This high efficiency design delivers up to 5A continuous current in boost mode (12A in buck mode). Only the inductor, sensing resistor, and bulk input and output capacitors are needed to finish the design. Figure 2 shows a typical LTM4605 application with an output of 12V at 5A. An optional RC snubber is added here to reduce switching noise for applications where radiated EMI noise is a concern.

Low Profile Solution

These power modules are offered in a space saving and thermally enhanced 15mm × 15mm × 2.8mm LGA package. This low profile package can fit the back side of PC boards for many high density point-of-load applications. Their high switching frequency and current mode architecture enable a fast transient response to line and load changes without sacrificing stability. Both can be frequency synchronized with an external clock to reduce undesirable frequency harmonics. Fault protection comes in the form of overvoltage protection and foldback current protection.

Smooth Transition and Circuit Simplicity

Both the LTM4605 and LTM4607 include the switching controller, four power FETs, compensation circuitry and support components. The 4-switch topology provides high efficiency in all three modes of operation—buck, buck-boost and boost—with a smooth transition between each.

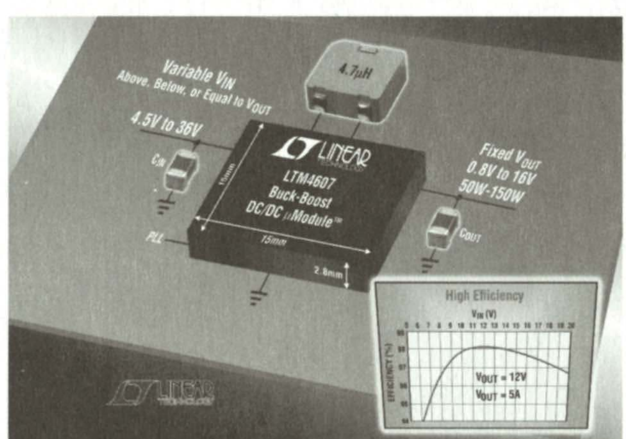

Figure 1. There is No Easier Way to Design a High Efficiency, High Power Density Buck-Boost Regulator than with the LTM4605 or LTM4607

Figure 2 shows an actual buck-boost design with external components chosen to satisfy the boost mode's 5A maximum load current. For buck-only applications, the maximum load current can be 12A at $12V_{OUT}$ with the same external components. For instance in a buck-only configuration, such as in Figure 3, the load current can be increased up to 7A at $12V_{OUT}$ for 168W capability. This application can achieve better than 98% efficiency as shown in Figure 4.

Excellent Thermal Performance

The low profile LGA package has a low thermal resistance from junction to pin (4°C/W), thus maintaining an acceptable junction temperature even when satisfying high power requirements. Typically, operation in room temperature ambient conditions requires no special heat sinking or added airflow, but for warmer ambient environments or high loads, simply add a heat sink to the top of the case for 2-sided cooling and add air flow to significantly lower the thermal resistance from junction to ambient. The data sheet provides more details about adding heat sinks and air flow considerations.

Conclusion

There is no easier way to design an efficient high-density buck-boost converter than with the LTM4605 or LTM4607 µModule regulator. No design tricks are necessary to achieve efficiencies up to 98%—only one inductor, a single sensing resistor and bulk capacitance are required to complete a design. Low profile LGA packages fit on the back side of PCBs and have good thermal performance, enabling a 168W power output in an 8cm × 8.4cm 4-layer PCB. These devices are ideal for automotive, telecom, medical, motor drive and battery-powered applications.

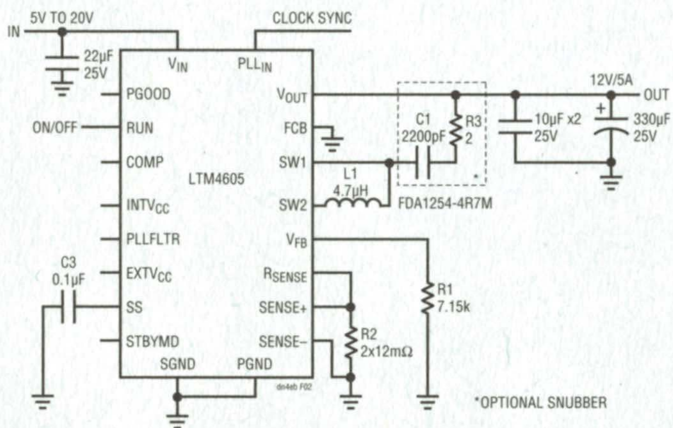

Figure 2. Buck-Boost Converter Produces $12V_{OUT}$ at 5A from a 5V to 20V Input Range

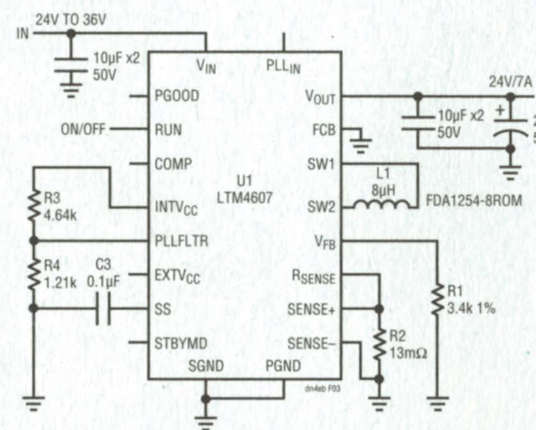

Figure 3. Buck Converter Produces a 24V Output with 168W Capability

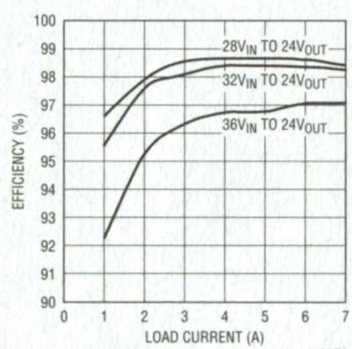

Figure 4. Efficiency for the $24V_{OUT}$ Converter in Figure 3

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Chop the noise gain to measure an op amp's real-time offset voltage

Glen Brisebois, Linear Technology, San Jose, CA

One of the most important specifications of an op amp is its input-offset voltage. You can null out this voltage on many op amps, but the problem with determining the input-offset voltage is that the offset voltage varies with temperature, flicker noise, and long-term drift. Chopping and autozeroing techniques have been around for several years, reducing achievable input offset to microvolts or less. The accuracy is so good that other minuscule effects, such as copper-solder thermocouple junctions, dominate the errors, until, with some effort, you can overcome them, as well. This Design Idea introduces a new type of chopping. "Chopping the noise gain" is a simple way to measure the offset voltage in real time, so that you can subtract it and enhance dc precision.

Figure 1 shows an LTC6240HV op amp in an inverting gain-of-10 configuration, along with several of its pertinent specifications. All of the input offset arrives at the output with a gain of 11 (called the "noise gain") as an output error. Any downstream circuitry or observer looking at the output voltage cannot distinguish the output error from the desired output signal.

Figure 2 shows the chop-the-noise-gain method. S_1 switches the additional shunt resistor, R_3, in and out, changing the noise gain without affecting the signal gain or bandwidth. There would normally be some degradation of bandwidth, but C_1 dominates the bandwidth limitation whether the switch is open or closed. Now, you impose a small square wave on the output with an amplitude that is equal to the present dc errors. You can demodulate out the error as with a conventional chopper, or you can subtract it in software in a modern ADC-based system.

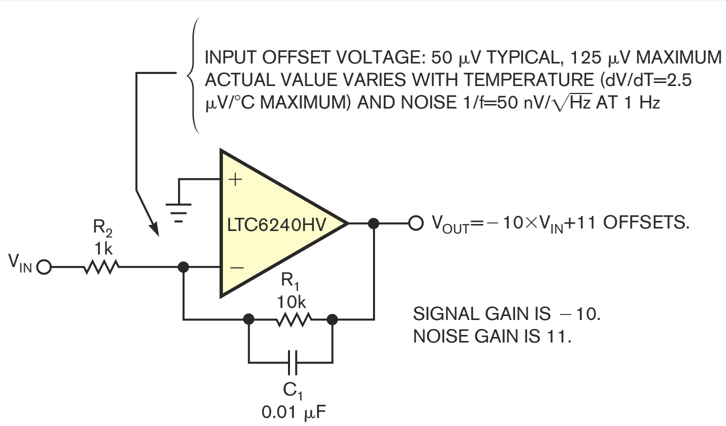

Figure 1 An op amp has a conventional gain of −10. The noise gain is 11, so all of the input errors appear at the output with a gain of 11. You cannot distinguish the signal from noise just by looking at the output.

DIs Inside

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The circuit in **Figure 2** is much like a simple summing amplifier, with one input both connected and disconnected. It is, in that sense, much like a true chopper amplifier. But, in this case, the input voltage being chopped is the amplifier offset, rather than the input signal. Why disconnect your input signal if you don't have to? Also, there is no need for continuous chopping; you need apply it only when you require an offset measurement.

Note that, although this Design Idea shows the inverting case for ease of understanding, the noninverting case is also practicable with a good analog switch for S_1. Also, as with any sampled system, frequencies at or greater than the clock rate alias into baseband, and you should therefore filter them out before the chopping. Finally, this method does not correct for bias- or leakage-current-induced errors.

Switch S_1 opens and closes, increasing the noise gain and imposing the input errors onto the output with alternating noise gains of 11 and 22. The resultant square wave now represents an easily measurable "11 errors," which you can then subtract from the output. This technique is similar to that of conventional chopper amplifiers, except that, in this case, you are chopping the error rather than the signal.

Figure 3 shows the oscillogram of the output of the circuit of **Figure 2**, with an input voltage of 0V (grounded). The top trace is "S," the control signal applied to S_1 at 750 Hz. The bottom trace is the output error alternating between 1 and 2 mV, indicating 90 µV of op-amp offset. The output "sees" the effect of doubling the noise gain of the output offset. The difference between the two noise gains is 11, and this difference dictates the amplitude of the square wave that S_1 causes, independently of the input voltage.

Figure 4 is similar to **Figure 3**, but zoomed out and with a 2-mV-p-p slow-moving sine wave signal at the input voltage—that is, 20-mV-p-p output. The 1-mV square wave of **Figure 3** is superimposed upon the slow-moving output signal and still contains the real-time dc-error information. Just by looking at the output, you can discern that the true value of the signal is 1 mV below the measured value. **EDN**

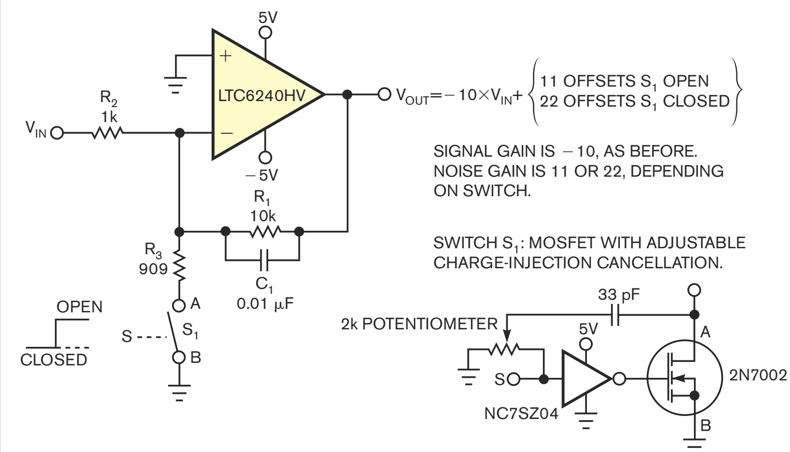

Figure 2 S_1 switches the additional shunt resistor, R_3, in and out, changing the noise gain without affecting the signal gain or bandwidth.

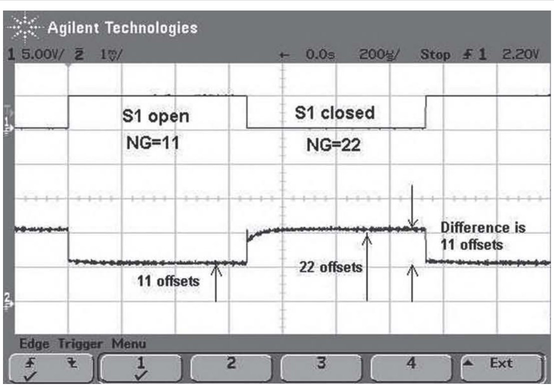

Figure 3 This oscillogram shows the output of the circuit in Figure 2, with an input voltage of 0V (grounded). The top trace is "S," the control signal applied to S_1 at 750 Hz. The bottom trace is the output error alternating between 1 and 2 mV.

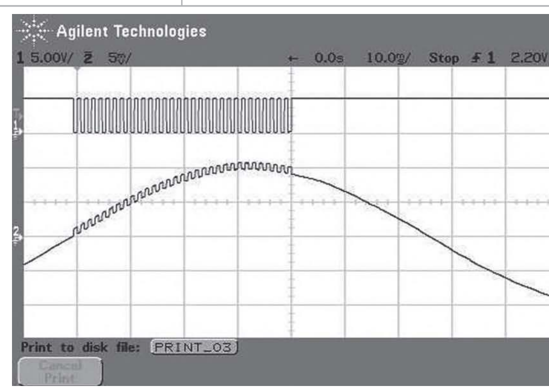

Figure 4 The oscillogram is similar to that in Figure 3, but with a 2-mV-p-p slow-moving sine wave signal applied at the input voltage.

Simple analog circuit provides voltage clipping and dc shifting for flash ADC

Alfredo del Rio, University of Vigo, Spain

Many flash ADCs, such as National Semiconductor's (www.national.com) ADC1175, have a recommended operating input-voltage range of 0.6 to 2.6V (**Reference 1**). However, in some applications, you must convert a symmetrical analog-input signal. The circuit in this Design Idea converts a symmetrical input-voltage range of −0.2 to +0.2V into the recommended 0.6 to 2.6V range (**Figure 1**).The circuit also prevents the output voltage from going below –0.3V, which would probably damage the ADC.

The circuit uses an Analog Devices (www.analog.com) AD8002 dual-current-feedback operational amplifier to obtain a high bandwidth (**Reference 2**). The first block, noninverting am-

plifier IC_{1A} has a voltage gain of five. This block also provides high input impedance and low output impedance, so that the second block, IC_{1B}, operates properly. The second block does most of the work. Starting from a basic inverting amplifier comprising IC_{1B}, R_4, and R_5, you obtain the clipping effect by adding R_3 and D_1. R_3, D_1, R_4, and R_5 determine the clipping level. In addition, adding the I_{DC} current dc-shifts the output voltage. You can trim adjustable potentiometer resistor P_1 to obtain the desired output voltage shift—that is, 1.6V.

If diode D_1's current is negligible, the output voltage, V_O, is $-(1+R_2/R_1)\times(R_5/(R_3+R_4))\times V_I+V_{CC}\times R_5/(R_6+P_1+R_7)=1.6-5\times V_I$. Given that the diode voltage, V_{DIODE}, is $0.6V_S$, $V_O=-(R_5/R_4)\times V_{DIODE}+V_{CC}\times R_5/(R_6+P_1+R_7)=1.6-1.65=-0.05V$.

The clipping takes place near 0V, protecting the ADC. Raising the clipping level makes the circuit less linear in the nonclipping range. In other words, a design trade-off exists between clipping level and linearity. Resistor R_8 limits the current through the ADC's input pin. Capacitor C_2 is optional; it limits the V_{ADC}/V_I bandwidth. Capacitor C_1 helps to reduce the voltage noise that might come from the $-V_{CC}$ power supply. EDN

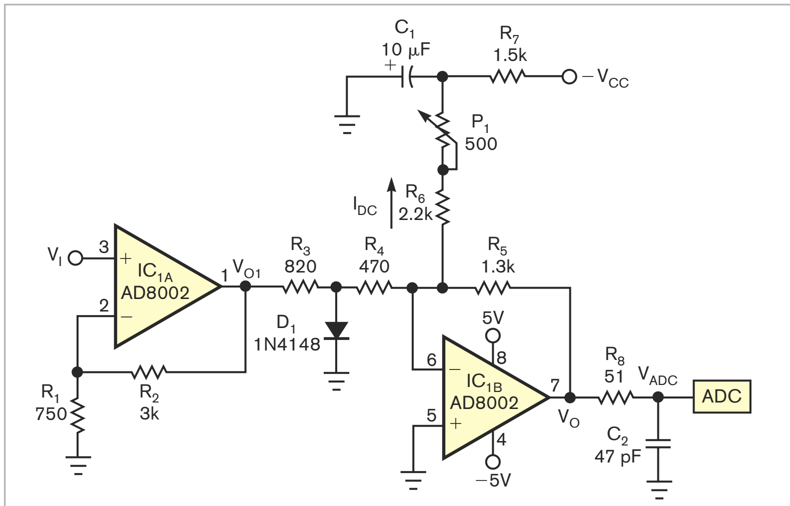

Figure 1 Adding R_3 and D_1 to a conventional op-amp circuit provides clipping. R_3, D_1, R_4, and R_5 determine the clipping level. In addition, adding the IDC current causes dc-shifting of the output voltage.

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2. "AD8002 Dual 600 MHz, 50 mW Current Feedback Amplifier," Analog Devices, www.analog.com/en/prod/0%2C2877%2CAD8002%2C00.html.

Compact laser-diode driver provides protection for precision-instrument use

Jiaqi Shen and Xiaoshu Cai,
University of Shanghai for Science & Technology, Shanghai, China

Continuous-wave laser diodes in precision-instrument applications require constant-current sources to drive them. Proper design of such a driver must involve careful tackling of robustness, stability, noise, and other issues and is consequently costly and complicated (**Reference 1**). **Figure 1** shows a compact, cathode-grounded laser-diode driver with protection against ESD (electrostatic-discharge) damage, start-up spikes, overshoot, and possible fluctuation arising from external optical feedback. An op amp, IC_4, with an enable input drives PMOS FET Q_1 and controls the output current. R_S sets the current to the rated value for a 35-mW HL6738MG laser diode from Opnext (www.opnext.com). To prevent output from Q_1 during start-up, comparator IC_{5A} keeps IC_4 off, and a 10-kΩ pullup resistor keeps Q_1 off by linking Q_1's gate to the supply of IC_4 until the terminal supply, V_B, reaches the designed value, approximately 6.5V, and opens Q_1 via IC_4.

The key point for protection against ESD damage and overshoot lies in the use of Q_2, a depletion-mode NMOS FET. With power off, Q_2 conducts, shunting any harmful ESD to ground. With power on, comparator IC_{5B} outputs a negative voltage far below the gate-to-source off-state voltage. Hence, Q_2 is off and has little effect upon the drive current unless the operating voltage at the laser's anode exceeds the maximum rating of 2.8V in the **figure**. In this case, the operating voltage triggers IC_{5B} to output high and thus turns on Q_2, shunting the drive current to ground, as well. The circuit now introduces significant hysteresis to latch off the state of emergency. Considering the low on-resistance of Q_2, this circuit provides better protection than the common method of relying on a paralleled zener diode for overshoot suppression (**Reference 2**).

Despite employing a split supply, this design requires no particular supply sequencing. You must cut off Q_2 only at the beginning of start-up, so it would be better to turn on the −9V external supply before enabling the driver. Despite the availability of substitutes for some ICs in this design, selection

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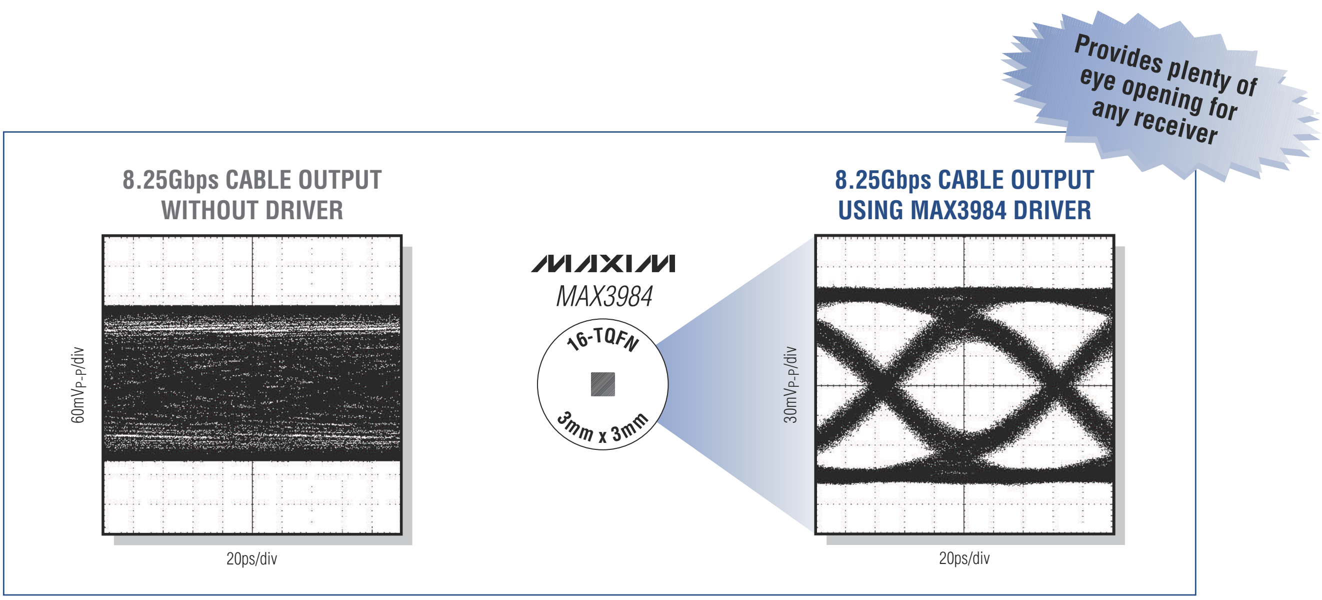

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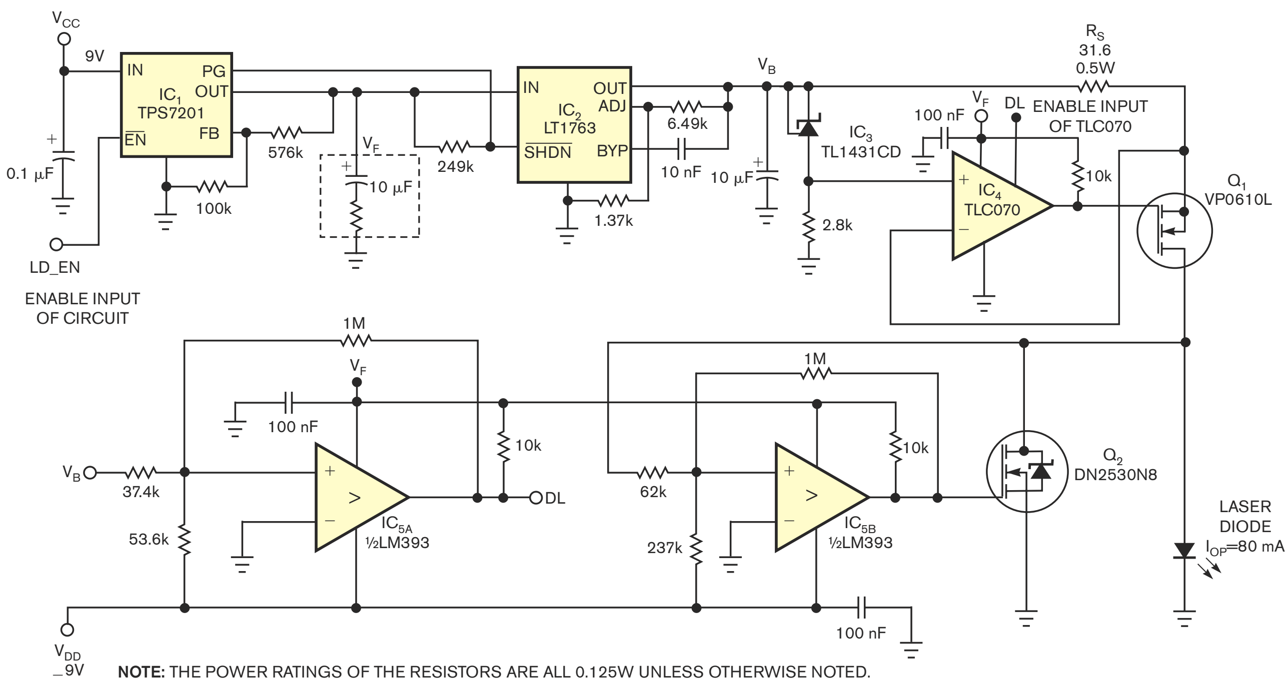

Figure 1 This laser-diode-drive circuit provides a constant current and protection against input overvoltages and start-up transients.

of the proper devices may be troublesome. For example, you can with slight modifications replace the Texas Instruments (www.ti.com) TLC070 with a Linear Technology (www.linear.com) LT1637; the two devices are not pin-compatible. However, the TLC070's superior ac performance, especially higher CMRR (common-mode-rejection ratio) over a wider bandwidth permits more effective protection against fluctuations in the operating voltage because of external optical feedback under some desired or undesired circumstances (**Reference 3**).EDN

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Current source makes novel Class A buffer

Horst Koelzow, Winnipeg, MB, Canada

The basis for this Design Idea is a classic two-transistor current source (**Figure 1**). Current through R_1 depends only on the V_{BE} (base-emitter voltage) of Q_2 and on the value of R_1 itself. The V_{BE} of Q_1 has no impact on the output current. Typically, this circuit finds use as a steady current source or as a limiter. The circuit forms the amplifier for the upper, positive half of the signal. Adding a complementary stage for the lower, negative half of the signal completes the buffer (**Figure 2**). The emitters of Q_2 and Q_3 become the input for the circuit, and the junction of sensing resistors R_1 and R_2 is the output. R_3 is an input-termination resistor that sets the output quiescent voltage. You can replace the bias sources (current

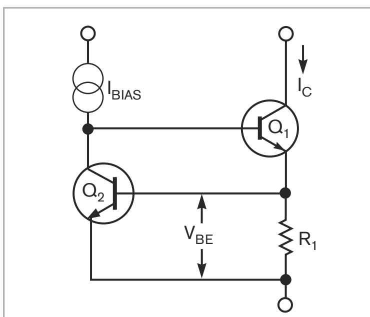

Figure 1 This classic two-transistor current source commonly finds use as a steady source of current or as a limiter.

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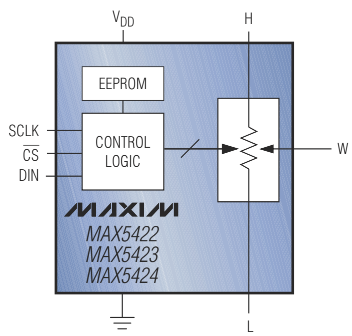

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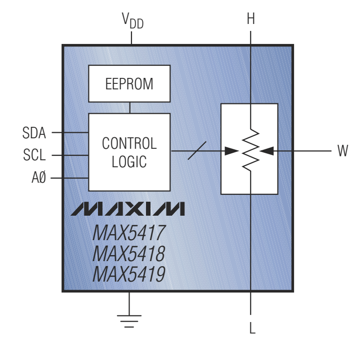
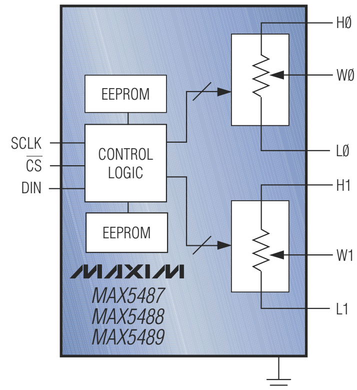
I²C



SPI



Dual

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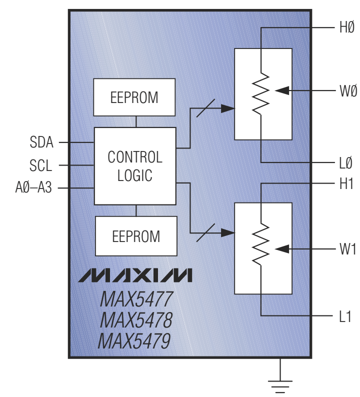
I²C



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sources in the **figures**) with resistors.

At the quiescent, 0V-input-voltage operating point, both halves of the circuit run at maximum current, and both the input and the output are at the same potential. When you impress a voltage on the input, you inject current into the Q_2-Q_3 emitter node. From there, current can go up into base of Q_1 or down into base of Q_4. The output voltage relative to the input voltage determines the direction of the injected current. If the input voltage is positive, it has no effect on the upper half because it is already limiting. It can, however, reduce drive current in the lower half, resulting in a reduction of lower output-drive current. Reduction of lower side output current results in a rise in output voltage. In short, an injected signal current "unlimits" the stage of opposite polarity.

At first glance, the circuit appears to have unity gain. But, because Q_2 and Q_3 sense the tops of R_2 and R_3 and not circuit output, R_1 and R_2 are effectively in series with the output load. If the load's impedance, R_{LOAD}, is small, the circuit gets significantly loaded down. However, as long as the input stage does not clip, the circuit does not become distorted. The source driving the buffer stage sets $h_{FE}(Q_1)\times(R_1+R_{LOAD})\Omega$, where h_{FE} is forward-current gain.

AN INJECTED SIGNAL CURRENT "UNLIMITS" THE STAGE OF OPPOSITE POLARITY.

Q_2 and Q_3 are common-base stages. Their purpose is to translate input voltage to the bias voltage that Q_1 and Q_4 require. This voltage-translation action allows direct substitution of other devices, such as MOSFETs or Darlington transistors.EDN

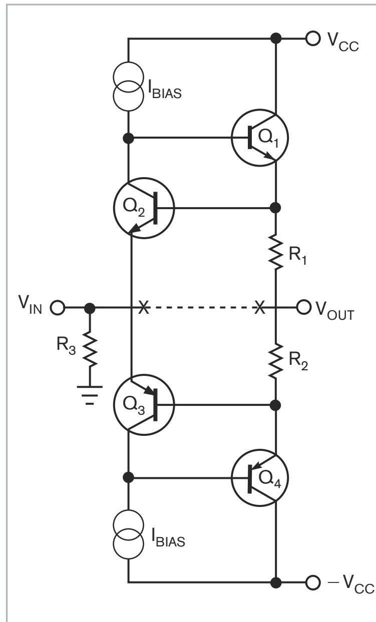

Figure 2 Adding another stage to the current source allows the circuit to function as a buffer.

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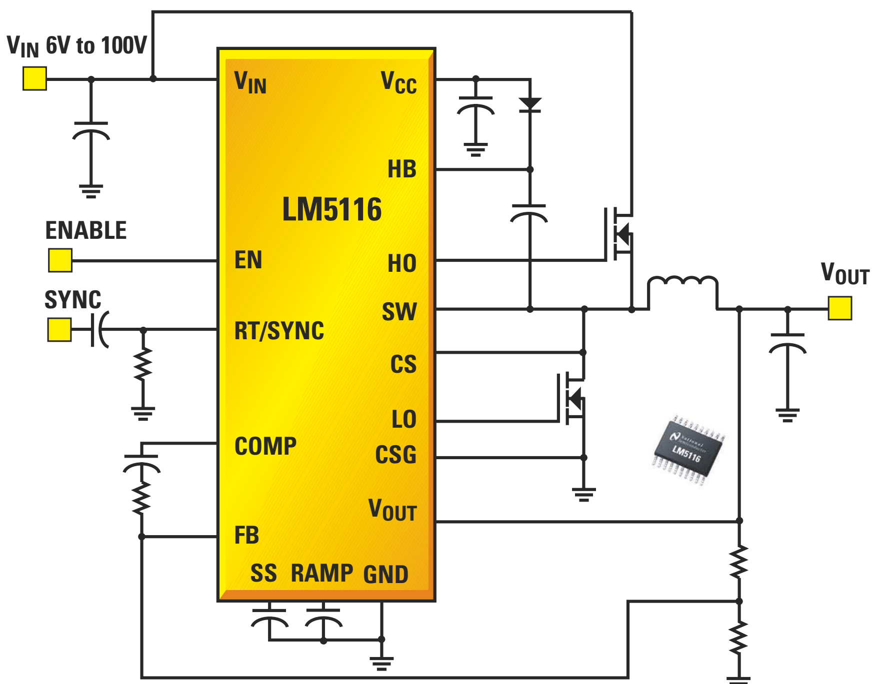

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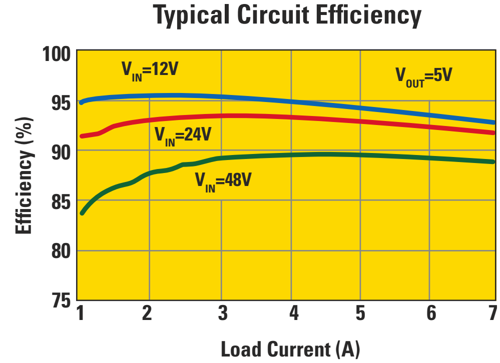

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LINKING DESIGN AND RESOURCES

Apple sneezes, flash industry gets sick

Demand cuts for NAND-flash memory from Apple Inc (www.apple.com) have driven down total NAND-market estimates for 2008. Reports from iSuppli Corp's (www.isuppli.com) industry sources indicate that the consumer-electronics maker significantly slashed its 2008 NAND-flash orders and has informed suppliers that its demand growth in 2008 will be slower than that of 2007. As a result, iSuppli reduced its outlook for 2008 global NAND-flash revenue growth to the single-digit-percentage range.

Before Apple's warning, iSuppli had predicted the company's NAND-flash purchases would rise by 32.2% this year, helping drive significant market growth. As proof of Apple's considerable impact on the NAND market, iSuppli points out that the company was the world's third-largest OEM buyer of NAND-flash memory in 2007, with purchases of $1.2 billion—13.1% of the global market.

The current economic situation, bearing the influence of the credit crunch and mortgage crisis, has weakened consumer spending. Sales to consumers drive NAND, which finds wide use in consumer-electronics applications, including flash-storage cards, MP3 players, and USB-flash drives.

The research company notes that slower NAND demand will have a major impact on suppliers' financial results. Indeed, capital spending on NAND production should increase by more than 20% this year. Such an increase would guarantee supply of parts and encourage average selling prices to decrease. ISuppli believes that NAND prices now are below suppliers' fully loaded costs.

"In light of these factors, NAND suppliers are likely to go into the red in the first quarter and are not likely to recover in the second," says Nam Hyung Kim (**photo**), director and chief analyst for memory at iSuppli. As 2008 shapes up to be a poor year for NAND, suppliers are likely to look back with nostalgia at 2007, when NAND revenue grew by 12.5% to reach $13.9 billion, iSuppli says.

GREEN UPDATE

EPA RELEASES ENERGY STAR GUIDELINES FOR SERVERS

The US EPA (Environmental Protection Agency, www.epa.gov) has released the first draft of its voluntary Energy Star (www.energystar.gov) power-efficiency specifications for computer servers. In doing so, the government agency has established its definitions of eligible server-product categories and laid the groundwork for later establishment of power-supply efficiency, power- and temperature-measurement, and power-management and -virtualization requirements that server manufacturers must meet to qualify their products as Energy Star-rated.

Load points of 10, 20, 50, and 100% are among the few technical points the draft establishes. The draft has so far declared a power factor only for the 100% load, at which the power factor will be 0.9. Although the EPA considers this power factor reasonable, the agency is reviewing whether the level will prove more challenging at lower loading points and will determine over the next few months whether the 10, 20, and 50% loads will need separate power-factor requirements.

The EPA is following its standard "tier" stepping process and will first introduce a Tier 1 set of Energy Star power efficiencies for servers and later increase requirements. The agency plans to work with industry groups over the next several months to test server supplies and create a real-world data set to develop consistent test procedures and efficiency levels. You can find the draft at www.energystar.gov/index.cfm?c=new_specs.enterprise_servers.

OUTLOOK

SUNNIER PROSPECTS FOR POLYSILICON

Frost & Sullivan (www.frost.com) expects the severe shortages and allocations of polysilicon, a key component of most solar panels, to turn around in 2008. The market-research company believes that polysilicon supply should catch up with the demand, offering sunnier prospects for the solar-energy industry. The majority of the new polysilicon quantities will come from four top suppliers that are expanding their production capacities. The big four—Hemlock Semiconductor, Renewable Energy Corp, Wacker, and Tokuyama—should add more than 17,000 tons of capacity in 2008, representing more than a 50% increase over their current capacities.

Frost expects demand from the semiconductor industry to grow at steady single-digit rates and demand for solar-grade polysilicon to reach more than 50% of the total demand for high-purity silicon in 2008/2009. Frost also reports that, in 2005, the global solar-photovoltaic market saw earned revenues of $6.49 billion. The company expects that figure to reach more than $16 billion in 2012, basing that prediction on a "huge demand" for polysilicon.

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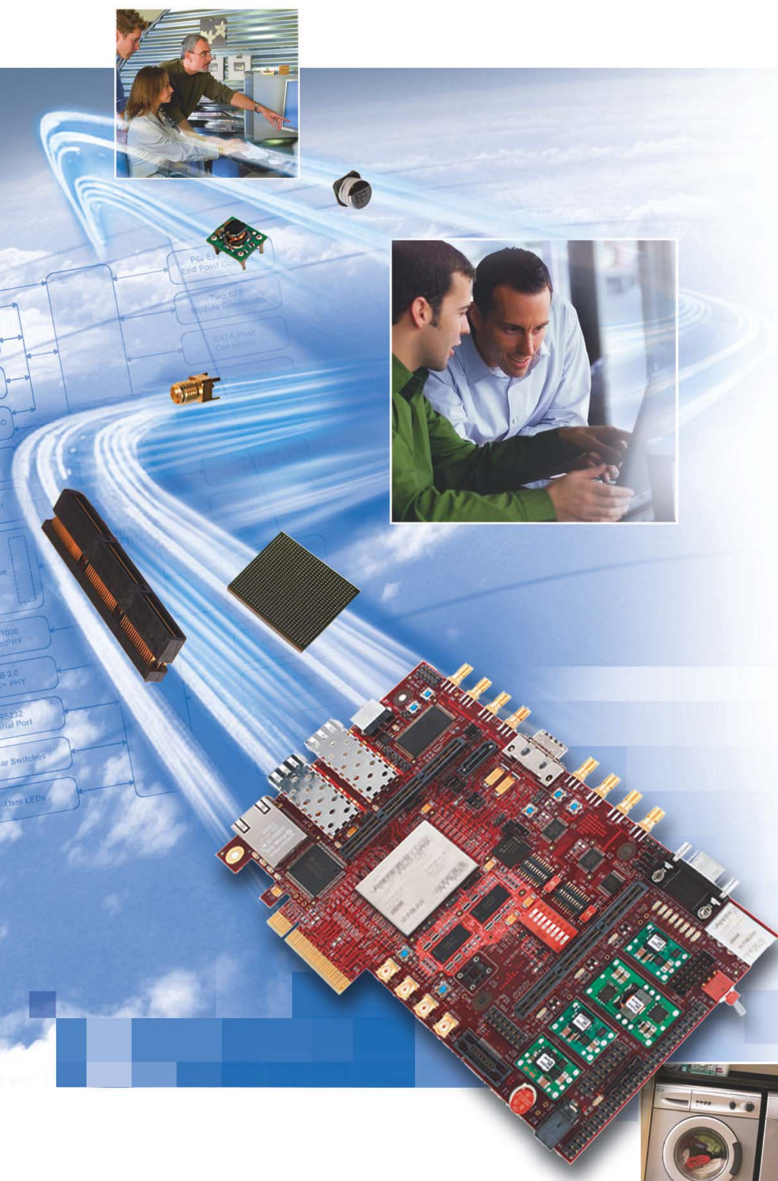

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productroundup

DISCRETE SEMICONDUCTORS

MOSBD devices integrate MOSFET, Schottky diodes

The TPCA8A02-H and TPCA8A03-H MOSBD (MOSFET/Schottky-barrier-diode) devices eliminate external wiring between the MOSFET and the diodes for increased power efficiency and reduce wiring resistance and inductance. The TPCA8A02-H features a 30V drain-to-source voltage with a maximum 34A drain current, and a 4.8-mΩ on-resistance; the TPCA8A03-H provides a 30V drain-source voltage with a maximum 15A maximum drain current, and a typical 5.1-mΩ on-resistance. The TPCA8A02-H comes in a 5×6×0.95-mm SOP, and the TPC8A03-H comes in a 5×6×1.6-mm SOP-8. The TPCA8A02-H and TPC8A03-H cost 55 and 50 cents, respectively.

Toshiba America Electronic Components, www.toshiba.com/taec

MOSFETs tout high efficiency

Suiting dc/dc converters, the STD60N3LH5 and STD85N3LH5 StripFET V Power MOSFET devices claim a superior performance and efficiency due to low on-resistance and lower total gate charge. The 30V devices offer an 8.8-nC gate charge, 7.2-mΩ on-resistance at 10V, and a figure of merit equal to on-resistance times gate charge. The STD85N3LH5 features a 4.2-mΩ on-resistance at 10V, and a 14-nC gate charge. Aiming at notebook-computer, server, telecom, and networking applications, the STD60N3LH5 and STD85N3LH5 costs 65 cents and 95 cents (2500), respectively.

STMicroelectronics, www.st.com

SOT883 MOSFETs take up 14% of PCB space

Taking up 14% of the PCB (printed-circuit-board) space, the SOT883-packaged MOSFETs claim a comparable power dissipation and performance to that of SOT23-packaged devices. Available in a 1×0.6×0.5-mm footprint, the MOSFET provides 0.65Ω on-resistance at 2.5V. The series features switching speeds of 12- to 16-nsec turn-on and 17- to 24-nsec turn-off. Prices for the PMZ760SN, PMZ390UN, PMZ250UN, PMZ270XN, and PMZ350XN start at 20 cents (10,000).

NXP Semiconductors, www.nxp.com

600V IGBTs reduce power dissipation

Targeting devices having 20-kHz switching and low short-circuit requirements, the 600V IRGB4059 IGBT (insulated-gate-bipolar-transistor) family reduces power dissipation by as much as 30%, according to the vendor. This reduction allows high-efficiency power conversion in UPS (uninterruptible-power-supply) and solar-inverter applications. With ultrafast soft-recovery diodes, the family provides lower collector-to-emitter saturation voltage and total switching energies than punch-through and non-punch-through IGBTs. The device also features internal ultrafast soft-recovery diodes improving efficiency and reducing EMI. The IRGB4059 IGBTs cost 68 cents.

International Rectifier, www.irf.com

Power MOSFET has low on-resistance

An advanced architecture and package design allow the NP180-

N04TUG power MOSFET to offer a 1.5-mΩ maximum on-resistance. Rated for single- and repetitive-avalanche energy, the power MOSFET operates at 175°C at a 10V gate voltage and a 40V drain-to-source voltage at a drain current of 180A. Available in ROHS (restriction-of-hazardous-substances)-compliant packages, the NP180N04TUG power MOSFET costs $2.50 (800).

NEC Electronics America, www.am.necel.com

900V superjunction MOSFET has low on-resistance

The 900V superjunction CoolMOS power MOSFET family suits SMPS (switched-mode-power-supply), industrial, and renewable-energy applications. The devices provide a figure of merit—mutiplying the on-state resistance by the gate charge—of 34V nC, resulting in low conduction, driving, and switching losses and in-

creased efficiency. The devices have 120-, 340-, or 1200-mΩ on-resistance and come in TO-246, TO-220, and D-PAK packages, respectively; 500-, 800-, and 1000-mΩ devices are available. The 120-mΩ TO-247 package costs $3.50.

Infineon Technologies, www.infineon.com

INTEGRATED CIRCUITS

High-definition-digital-TV platform has worldwide-standard support

Based on the vendor's STi1010 single-chip IDTV (integrated-digital-television) processor, the DTV50 single-chip, high-definition decoder-and-processor platform supports worldwide standards. The platform features demodulation, MPEG-2 high-definition- and standard-definition-decoding, high-definition-video-processing, high-quality-audio, and video-switching functions for IDTV sets worldwide. Using STi101X processors, the STi1010 provides high-definition-display capabilities with a picture-in-picture feature, and the STi1011 suits the WXGA (wide-extended-graphics-array) version with no picture-in-picture feature. Available in a 27×27-mm PBGA package, the DTV150 platform with a high-definition configuration costs $45.

STMicroelectronics, www.st.com

Video decoder has 3-D NTSC/PAL comb filter

Combining a 12-bit 3-D comb filter with 1080p-high-definition and 150M-sample/sec sampling rate, the ADV7802 video decoder provides 4:4:4 sampling throughout the processing pipeline, including support for RBG SCART (Syndicat Français des Constructeurs d'Appareils Radio et Télévision) inputs. An on-chip interface with SDR (single-data-rate) DRAM reduces system cost, and DDR (double-data-rate) DRAM support enables simultaneous 12-bit NTSC/PAL (National Television System Committee/phase-alternation-line) 3-D comb, DNR (digital-noise reduction), and TBC (timebase correction). Available in a TQFP-176 package, the ADV7802 video decoder costs $12; the ADV7800 10-bit version costs $10.

Analog Devices, www.analog.com

Triple-core processor has an audio engine and a security processor

Aiming at 1024-bit and greater encryption techniques, the DM870 ARM9-based triple-core processor provides a dedicated audio engine, a real-time tamper-resistant security processor, and integrated wireless-Internet support. The 240-MHz ARM926EJ processor core supports Linux, MP3, WMA, AAC, and other audio-decompression standards and offers generous additional processing bandwidth for system control and advanced user-interface operations. Targeting use in complex-audio processing, the audio engine supports real-time MP3 encoding and WMA (Windows-media-audio) lossless decoding. Additional features include support for popular sound-enhancement algorithms; 600-MIPS computational power; and on-chip Ethernet-, wireless-Internet-, and USB-interface connectivity options. The processor integrates 802.11a/b/g MAC (media-access control), an internal color-LCD controller, and onboard stereo-PWM (pulse-width-modulation) outputs. Measuring 17×17-mm in an mBGA-292 package, the DM870 processor costs $14 (1000) bundled with the JukeBlox SDK (software-development kit). The JukeBlox development platform includes a hardware-reference platform and an SDK and costs $10,000.

BridgeCo, www.bridgeco.com

Automotive-contact monitors maintain eight remote switches

The MAX13037/MAX13038 automotive-contact monitors and level shifters provide an integrated voltage regulator, a watchdog timer, and reset functions. The devices monitor and debounce eight remote mechanical switches and consume 28-μA typical supply current using programmable polling periods and a programmable scanning period. Aiming at harsh automotive environments, such as body-controller applications, the devices feature a ±45V input-voltage range, ±8-kV ESD protection on switch inputs, adjustable wetting current, and low dropout. An open-drain interrupt output is active in the absence of a logic supply and can wake up external microcontrollers from a sleep state. An SPI (serial-peripheral interface) reads the switch status and configures the operating characteristics of each device, and the switch inputs provide programmable wetting current and switching hysteresis. Four inputs allow ground-connected switches, and the other four inputs are programmable in groups of two as battery- or ground-connected switches. The microcontroller-interface pins are configurable to direct-level-shifting outputs for interfacing with PWM (pulse-width-modulation), low-voltage, or other timing signals. Operating over 6 to 26V battery voltage and withstanding a 42V load dump, the contact has a 2.7 to 5.5V logic-supply input that sets the interface voltage. The device has a −40 to +125°C automotive-temperature range. The MAX13037 features a 5V low-dropout regulator, and the MAX13038 has a 3.3V low-dropout regulator; both low-dropout devices provide 150 mA. Available in a 6×6-mm, ROHS (restriction-of-hazardous-substances) TQFN package, the MAX13037/MAX13038 automotive-contact monitor and level shifter cost $2.16 (1000) each.

Maxim Integrated Products, **www.maxim-ic.com**

2V-rms audio-line driver operates from 3.3V power supply

Operating from a 3.3V power supply, the DRV601 2V-rms DirectPath audio-line driver adjusts input-gain levels. The device integrates a charge pump and has a 1.8 to 4.5V power-supply range and independent right- and left-channel-shutdown control. The device also includes short-circuit and thermal protection, pop-reduction circuitry, and a 105-dB dynamic range. Available in a 4×4-mm QFN package, the DRV601 audio-line driver costs 90 cents (100).

Texas Instruments, **www.ti.com**

Audio-DSP kit uses Symphony Studio software

The Symphony Studio software and the Symphony SoundBite audio-DSP kit allow developing, debugging, and simulating applications using an IDE (integrated-development environment). Using the open-source Eclipse platform, Symphony Studio software works with the vendor's audio DSPs, including the multicore DSP5672x devices. The kit suits cost-sensitive applications, independent-design houses, small development shops, and college laboratories. Shipping with the vendor's Symphony DSPB56371 DSP on a form-factor PCB (printed-circuit board) with a 256-kbyte serial EEPROM, the device also includes a mini-USB interface and DIP switches for user inputs. The kit also includes an evaluation board, a mini-USB cable, and a CD-ROM with software and start-up documentation. Available for downloading from the vendor's Web site, the Symphony SoundBite development kit costs $150.

Freescale Semiconductor, **www.freescale.com**

QVGA modules have RO8803 controller

The 5.7-in. monochrome STN (supertwisted-nematic) and FSTN (film-compensated-STN) QVGA modules come in FSTN gray, positive, and transflective or STN blue, negative, and transmissive configurations. The devices are available with an RO8803 controller with built-in touchscreen controller with CCFL (cold-cathode-fluorescent-lamp) or LED backlighting. The STN negative blue-mode module CCFL backlight costs $42.50 (1000) or $39.87 (5000).

Phoenix Display International, **www.phoenixdisplay.com**

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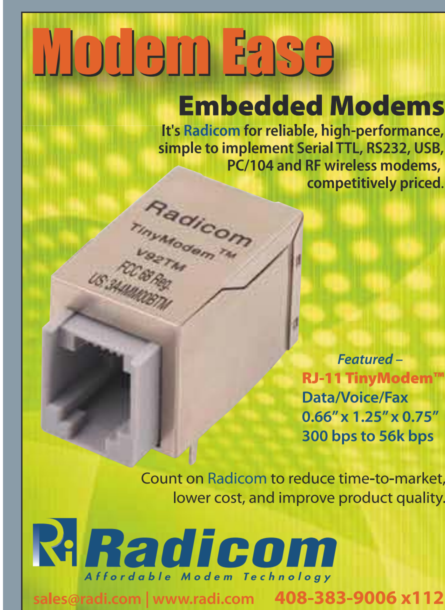
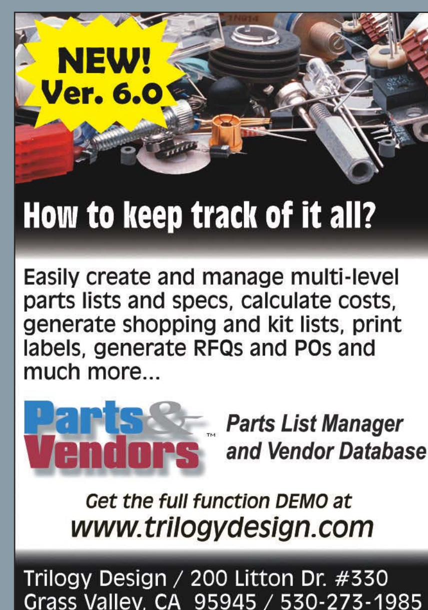
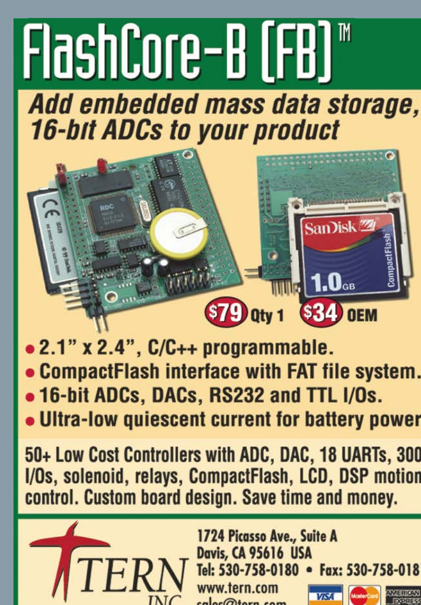






BY MARTIN DELATEUR • CONSULTANT

Contamination: not your usual suspects

DANIEL VASCONCELLOS

While working in the 1980s for a major semiconductor manufacturer, we had a major yield problem that was baffling the production team. Yields were decreasing on a daily basis because of high leakage failures. The usual suspects in this case are positive ions (sodium) or heavy-metal contamination causing leakage in the oxide layers. Sources for these ionic contaminants can range from a defective dopant bottle to a bag of chips an operator sneaks into the fabrication facility. We applied all the usual approaches to correcting the problem, including changing diffusion sources and cleaning all the glassware, and the yields improved.

We used CV (capacitance-versus-voltage) plots to determine that heavy metal was the source of the decrease in yields and determined that, after cleaning, we had eliminated the source. Unfortunately, only a week later, the problem returned. The CV plots once again confirmed the presence of heavy metal. The next step was to replace all the large, expensive quartz tubes in the diffusion oven. Wafers sat in these tubes while the oven heated and diffusion gases flowed over the wafers. Replacing these tubes upset the production-team members, but they felt that they had at least cured the contamination problem.

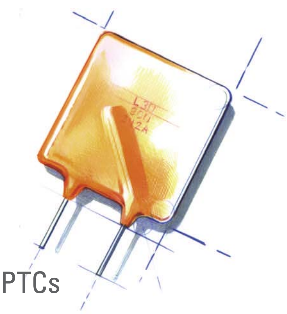
The transistors inside the new quartz tubes were good ones and met all the specifications. Everything was fine for three months. Then the exact same problem developed again. Transistor yields plunged, and it seemed that heavy metal was again the problem. The team ran many experiments and tried several approaches to determine the source of the contamination. Investigations found that there was gold in the silicon and that it was ruining the electrical properties. When you use gold in high-speed switching transistors, it provides a place for hole-electron pair recombination, speeding transistor switching. For linear transistors, however, the gold just ruins the properties with excessive leakage and poor low-current amplification. But the investigators thought that they had eliminated any and all potential sources of gold contamination.

After some extensive research on what had changed in the fab, they found that the fab had brought in a used diffusion oven from another division. The diffusion oven had come from a line that was making high-speed chips, and that other line had at one point used the oven for gold diffusion. Changing glassware was not permanently solving the problem. If gold could diffuse into the quartz tubes, it could also continue on and contaminate the heating coils. We got a new set of quartz tubes and also changed the heating coils.

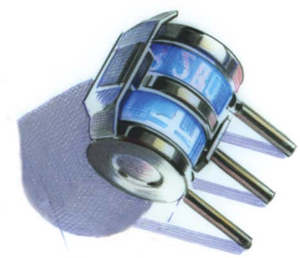
Even after three months, the transistors coming out of that furnace were just fine. It turns out that, in the old factory, the gold had continued to diffuse into the quartz. When the gold atoms reached the outside of the quartz tube, they deposited themselves on the nichrome heating coils. It had taken three months for the gold to diffuse from the outside to the inside of the tubes; it then began to ruin the wafers inside the tubes. This fact amazed the production people, but anyone who has worked on semiconductor processes knows that you can never just look at the usual suspects. EDN

Martin DeLateur is a consultant who spent 30 years as a product engineer at Fairchild and National Semiconductor. Contact him at delateurm@all2ez.net. Like Martin, you can share your Tales from the Cube and receive $200. Contact edn.editor@reedbusiness.com.

Varistors



PTCs



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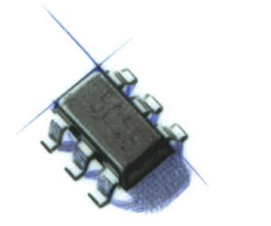

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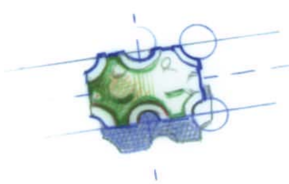

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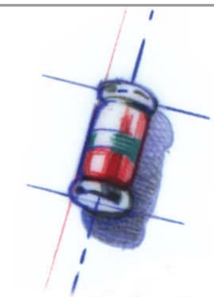

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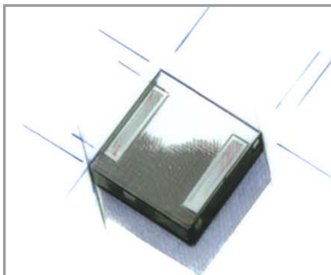

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